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VOICE OF THE ENGINEER

APRIL 17
Issue 8/2008
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EMBEDDED TECHNOLOGY

DESIGNERS CHOOSE FROM THE LATEST FABRICS

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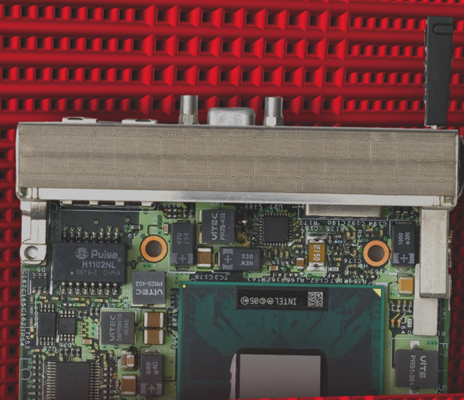

INTEGRATING HIGH-SPEED SERIAL I/O: no snap for SOC designers

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Blind prefetching improves PCI Express-to-PCI-bridge performance

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HOW TO MAXIMIZE APPLICATION PAYLOAD WITH A MINIMAL MACHINE-CODE FOOTPRINT

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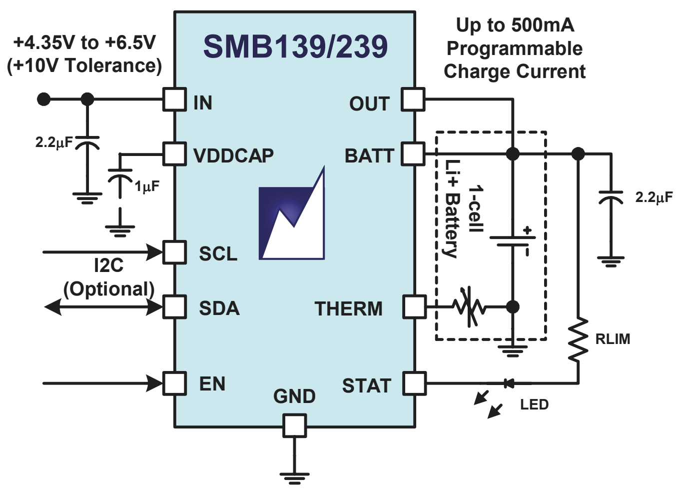
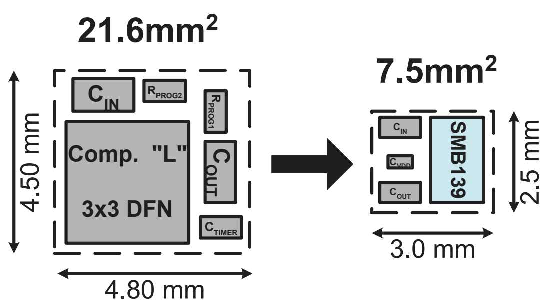


Shrink Solution Size by 65% vs. Existing Chargers



SMB139/239 Applications

- Bluetooth™ phone headsets
- Bluetooth™ stereo headphones
- Ultra-thin phones/media players
- Wristwatch GPS/MP3
- Sports/wearable electronics
- Portable biometric monitors

Summit's Family of Programmable Battery Chargers The Ideal Solution for Your Portable Application

	SMB137	SMB138	SMB135/235	SMB139/239
Topology	Switch-mode	Switch-mode	Switch-mode	Linear-mode
Input Voltage Range (V)*	4.35 to 5.5 (16)	4.35 to 6.0 (16)	4.35 to 6.5 (10)	4.35 to 6.5 (10)
# of Inputs/Outputs	2/2	1/1	1/1	1/1
Maximum Charge Current (mA)	1500	1250	900	210/500
TurboCharge™ Output	Automatic	Automatic	Software/uC	
CurrentPath™ Control	X			
USB On-The-Go Power	X	X		
Low-Battery Recovery Mode	X			
I2C Interface	X	X	X	X
Programmable Float Voltage	X	X	X	X
Programmable Charge/Term. Current	X	X	X	X
Programmable Input Current Limit	X	X		
Input/Battery OV/UV	X	X	X	X
Hardware Safety Timer	X	X	X	X
Software Watchdog Timer	X	X		
Battery Thermal Protection	X		X	X
IC Thermal Protection	X	X	X	X
Package	3.6x3.3 CSP-30	3.1x2.1 CSP-20	2.1x1.3 CSP-15 5x5 QFN-32	2.1x1.3 CSP-15 5x5 QFN-32
Solution Size (mm2)	50	28	31	7.5

* () Indicates overvoltage "holdoff" tolerance

For more information see:
www.summitmicro.com/SMB139

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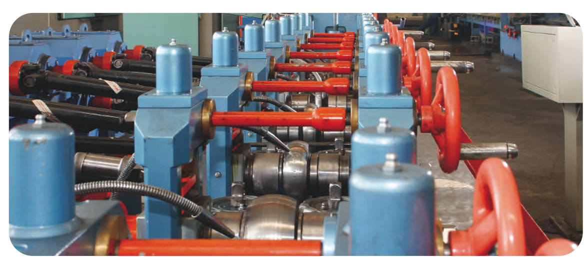

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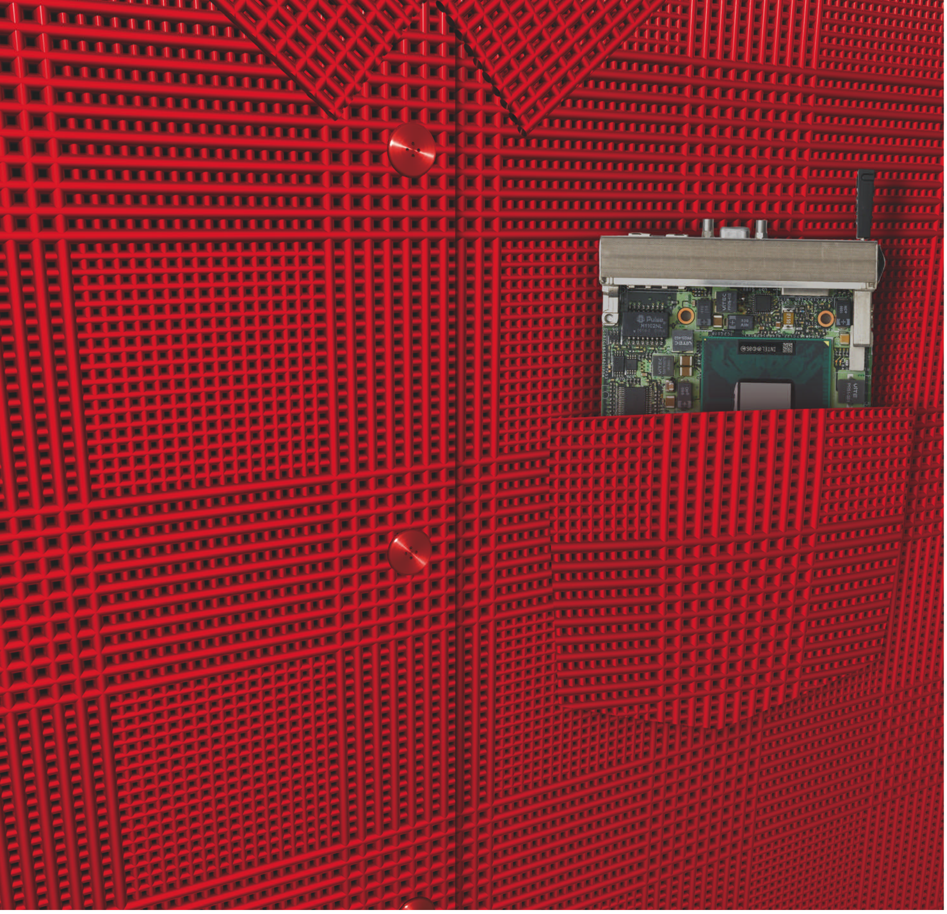

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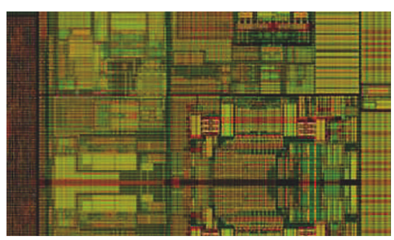
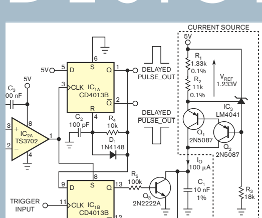


DESIGNIDEAS



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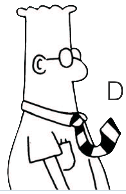
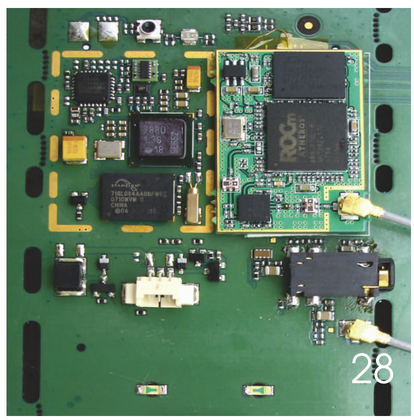
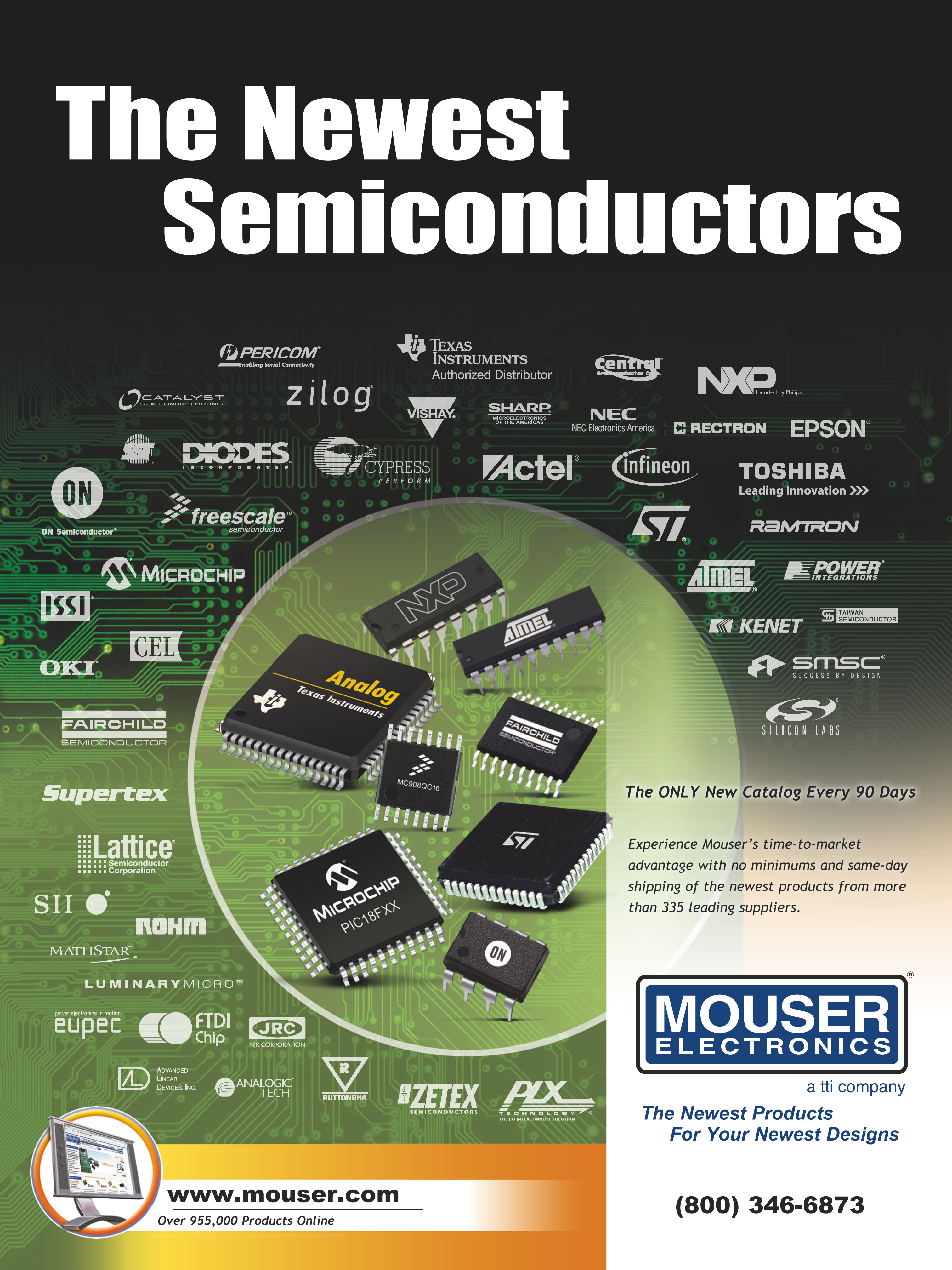




DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

EDN® (ISSN#0012-7515), (GST#123397457) is published biweekly, 26 times per year, by Reed Business Information, 8878 Barrons Blvd, Highlands Ranch, CO 80129-2345. Reed Business Information, a division of Reed Elsevier Inc, is located at 360 Park Avenue South, New York, NY 10010. Tad Smith, Chief Executive Officer; Mark Finkelstein, President, Boston Division. Periodicals postage paid at Littleton, CO 80126 and additional mailing offices. Circulation records are maintained at Reed Business Information, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. Telephone (303) 470-4445. POSTMASTER: Send address changes to EDN®, PO Box 7500, Highlands Ranch, CO 80163-7500. EDN® copyright 2008 by Reed Elsevier Inc. Rates for nonqualified subscriptions, including all issues: US, $165 one year; Canada, $226 one year, (includes 7% GST, GST#123397457); Mexico, $215 one year; air expedited, $398 one year. Except for special issues where price changes are indicated, single copies are available for $10 US and $15 foreign. Publications Agreement No. 40685520. Return undeliverable Canadian addresses to: RCS International, Box 697 STN A, Windsor Ontario N9A 6N4. E-mail: Subsmail@ReedBusiness.com. Please address all subscription mail to EDN®, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. EDN® is a registered trademark of Reed Elsevier Properties Inc, used under license. A Reed Business Information Publication/Volume 53, Number 8 (Printed in USA).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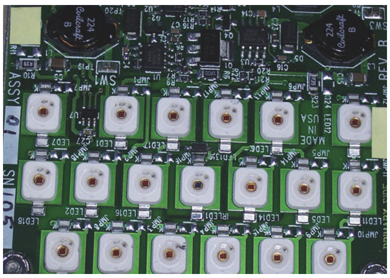

ONLINE ONLY

Check out these Web-exclusive articles:

Designing with high-power LEDs on epoxy-glass boards
Learn the fundamentals of thermal design and how it can be implemented using practical methods and materials to produce acceptable high-power LED applications.
→www.edn.com/article/CA6545911

Regulatory commissions sound off about acoustic shock
Recently implemented European directives require employers to protect workers from the dangers of acoustic shock. Read on to understand the issue and the technical challenges.
→www.edn.com/article/CA6545956

A few useful formulas for magnetic-products design
These useful equations assist in selecting magnetic cores, making the necessary gap assessment, determining magnetic-core parameters, and evaluating the energy-storage capability of gapped cores.
→www.edn.com/article/CA6545406

Wanted or not, H-1B visa process begins
Do you care if your company doesn't get all the visas it wants?
→www.edn.com/080417toc1

Ansoft releases target high-speed-circuit and electromagnetic design
Ansoft has announced new releases of its Nexxim high-capacity circuit-simulation software and Ansoft Designer integrated schematic and design-management software.
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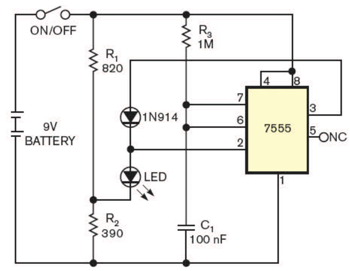


READERS' CHOICE

A selection of recent articles receiving high traffic on www.edn.com.

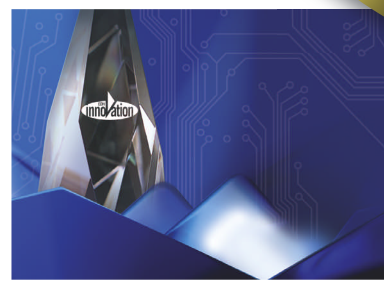
Red LEDs function as light sensors
You can build simple LED illuminators using the red LED to sense ambient-light level.
→www.edn.com/article/CA6541376

Precision voltage-controlled current sink tests power supplies
A simple voltage-driven current sink allows you to test the dynamic behavior of power supplies.
→www.edn.com/article/CA6541375

Genetic algorithm solves thermistor-network component values
An algorithm employing survival-of-the-fit-test principles finds the optimal resistor and NTC thermistor values for applying temperature compensation to an active device.
→www.edn.com/article/CA6542464

Harvest energy using a piezoelectric buzzer
You can harvest small amounts of mechanical energy using a piezoelectric buzzer to charge a supercapacitor.
→www.edn.com/article/CA6541379

Flyback transformer enables high power factor and converter efficiency
Ever-tightening regulations require a power factor of at least 0.9 and high efficiency for offline power supplies. This new switching-converter topology uses a flyback transformer and accomplishes both these goals in one stage.
→www.edn.com/article/CA6535349



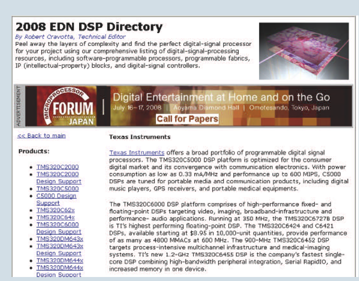
INNOVATION AWARDS

***EDN* CROWNS INNOVATION AWARD WINNERS**
EDN announced the Innovator of the Year and the Innovations of the Year at an awards ceremony on April 14. Find out who took home top honors.
→www.edn.com/innovation18

FROM *EDN'S* BLOGS

Joost's live test: No antenna? No coax? No fiber? No problem
From Brian's Brain, by Brian Dipert

Internet-delivered television content, advertising-supported (therefore free), with no IPTV subscription required? Looks and sounds good to me. What about you?
→www.edn.com/080417toc3



FIND YOUR DSP

The online version of *EDN*'s 2008 DSP Directory—a drastically expanded version of what appeared in these pages last month—is now available. The directory allows you to quickly home in on DSP devices and cores that meet your application needs.
→www.edn.com/dspdirectory

QuickLogic Introduces VEE:
The Visual Enhancement Engine – Delivering the next generation in mobile entertainment experience

VEE enables a TV-quality visual experience on mobile devices while dramatically reducing the LCD backlight to improve battery life

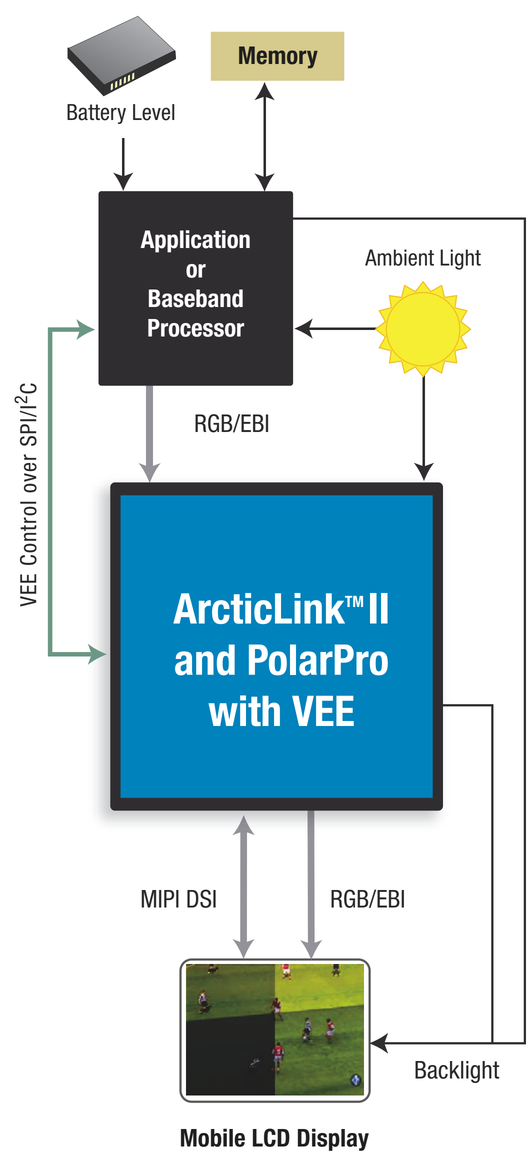
These three Use Cases illustrate how QuickLogic's proprietary VEE solution greatly enhances image and video quality by dynamically compressing the display range to match the characteristics of the LCD, with the intended viewing experience of the source content, resulting in a substantially better viewing experience under any conditions.

VEE technology transforms the mobile multimedia experience by:

- Significantly enhancing image/video quality through dynamic range control
- Allowing superior viewing image/video quality under low backlight or bright ambient light conditions

Multimedia Trends – User Experience
The multimedia user experience has become one of the key selection criteria for the handset market because its success is essential to the adoption and growth of emerging technology aimed at increasing network operator revenues. True mobility inherently means that a device must be able to provide this unique user experience under any condition consumers will be in—on trains, planes, in bright sunlight, in the dark, tethered to wall power or completely unplugged.

VEE Technology – The Answer
Stringent design requirements are placed squarely on the shoulders of the OEMs and ODMs that supply products to the consumer market. One limitation these OEMs and ODMs have is how mobile displays often truncate the effective contrast of the content con-sumers are viewing on their mobile devices. QuickLogic is addressing this challenge with a new technology called the Visual Enhancement Engine (VEE). The patented, proven VEE technology supplies high quality contrast optimiza-tion for a wide range of mobile consumer and prosumer devices, providing consumers with a TV-quality viewing experience while, at the same time, extending battery life.



Use Case 1 – Improved Video Quality

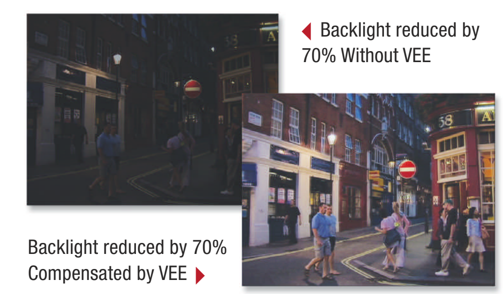
A commuter goes from a train station to outdoors, while watching a movie, with backlight automatically compensated.

One benefit of VEE's visibility improvements is that the mobile device does not require a powerful backlight in order to provide daylight viewing. The enhancement engine will compensate for the display's reduced contrast, ensuring a consistent high-quality viewing experience despite lighting changes.

Use Case 2 – Battery Life Extension

A traveler low on battery power can now finish a two-hour movie while on an airplane because VEE automatically adjusts in real time to compensate for reduced backlight.

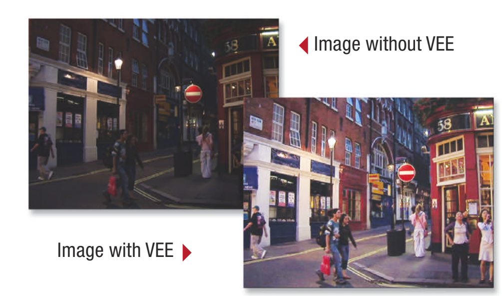
With traditional display technology, developers have only two options for overcoming viewability concerns. One is to increase backlighting, particularly in high ambient light conditions. However, for mobile device designers, this option has a serious drawback—increased power consumption. The backlight for a mobile display consumes between 30% and 60% of the device's power budget. The VEE technology from QuickLogic automatically compensates for the reduced backlight thus increasing battery life, while providing a satisfactory viewing experience.



Use Case 3 – Enhanced Still Pictures

A tourist takes a picture while sightseeing and can now see the detail captured in the picture on the built-in LCD display. These details would normally be lost due to the limited contrast ratio of these LCDs. With VEE, the details are now visible, reassuring the tourist that their vacation is being accurately captured.

The VEE enhancements arise from the re-mapping of image data to amplify subtle variations and make them more apparent to the eye. This image-dependent remapping addresses display limitations in two ways. First, it ensures that image details are preserved against truncation by the display's limited input range. Second, by taking into account the surrounding data values, the mapping enhances image detail in light and dark image areas appropriately.



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BY WARREN WEBB, TECHNICAL EDITOR

Those devilish details

Embedded-system designers are once again emerging from their cubicles and laboratories to saunter up and down the aisles of the Silicon Valley version of the Embedded Systems Conference in search of the latest products and techniques to ease their professional lives. No, you won't see the end products that these designers are famous for, such as medical instrumentation, industrial automation, military-weapon systems, or even the latest portable-multimedia devices. What you see are the hidden details that designers use to make these products perform their magic. Embedded design is all about sufficiently defining and controlling these details to produce the desired result within budget and on schedule.

But what exactly are these embedded-system designers looking for at a gathering such as the Embedded Systems Conference? They are looking for the elusive component that will eliminate the noise or increase the bandwidth of the project's latest circuit design. They want low-cost debugging tools that will reduce all of those hours spent locating that last bug in the firmware. They also want an educational or how-to seminar to get them up to speed for the extreme expectations of the next project. They need the embedded details that will guide them along a successful path in their career. Or maybe they just want a little time away from the office.

One embedded-system detail has a major impact on embedded design: the industry's transition from a parallel-multidrop-bus structure to switched-serial-fabric interconnections. We have dedicated this issue to the ins and outs of fabric technology at both the board- and the chip-design levels. My cover story outlines the latest board-level-interconnection strategies you need to keep up with the soaring data rates in today's embedded systems. I also examine several ways that board standards integrate the new switched fabrics into legacy technology to reduce costs and simplify the transition. Taking high-speed serial technology one level deeper, *EDN*'s Executive Editor Ron Wilson uncovers switched fabric's impact on system-on-chip designs. Ron discusses the integration of high-speed serial I/O—from IP (intellectual-property)-vendor selection through the integration and verification processes.

We have dedicated this issue to the ins and outs of fabric technology at both the board- and the chip-design levels.

April is also that time of year when *EDN* honors the creators of the hottest product, software, and technical articles deemed most valuable to the embedded-design community. Our annual *EDN* Innovations Awards ceremony honors outstanding engineering professionals and the products they conceive. This year's product finalists include a diverse list of embedded details, including a video-format converter from Marvell, an industrial ADC from Cirrus Logic, and a wireless-development tool from Texas Instruments. We announced the winners on April 14. *EDN* donates a portion of the proceeds from the nominations and the awards event to an engineering college or university that the Innovator of the Year chooses. It's our way of encouraging and supporting tomorrow's great minds. You can find a complete listing of the finalists and winners at www.edn.com/innovation.

As you marvel at our industry's electronic masterpieces, you can be sure of one thing: A team of embedded-system designers painstakingly analyzed and tuned all of the minute hardware and software details. And the next time you hear the hackneyed phrase "the devil is in the details," I hope it will remind you of embedded-system-design engineers and their daily trek through our industry's electronics minutiae to stretch the technology envelope to fit their current project assignments.**EDN**

What are your thoughts? Contact me at wwebb@edn.com.

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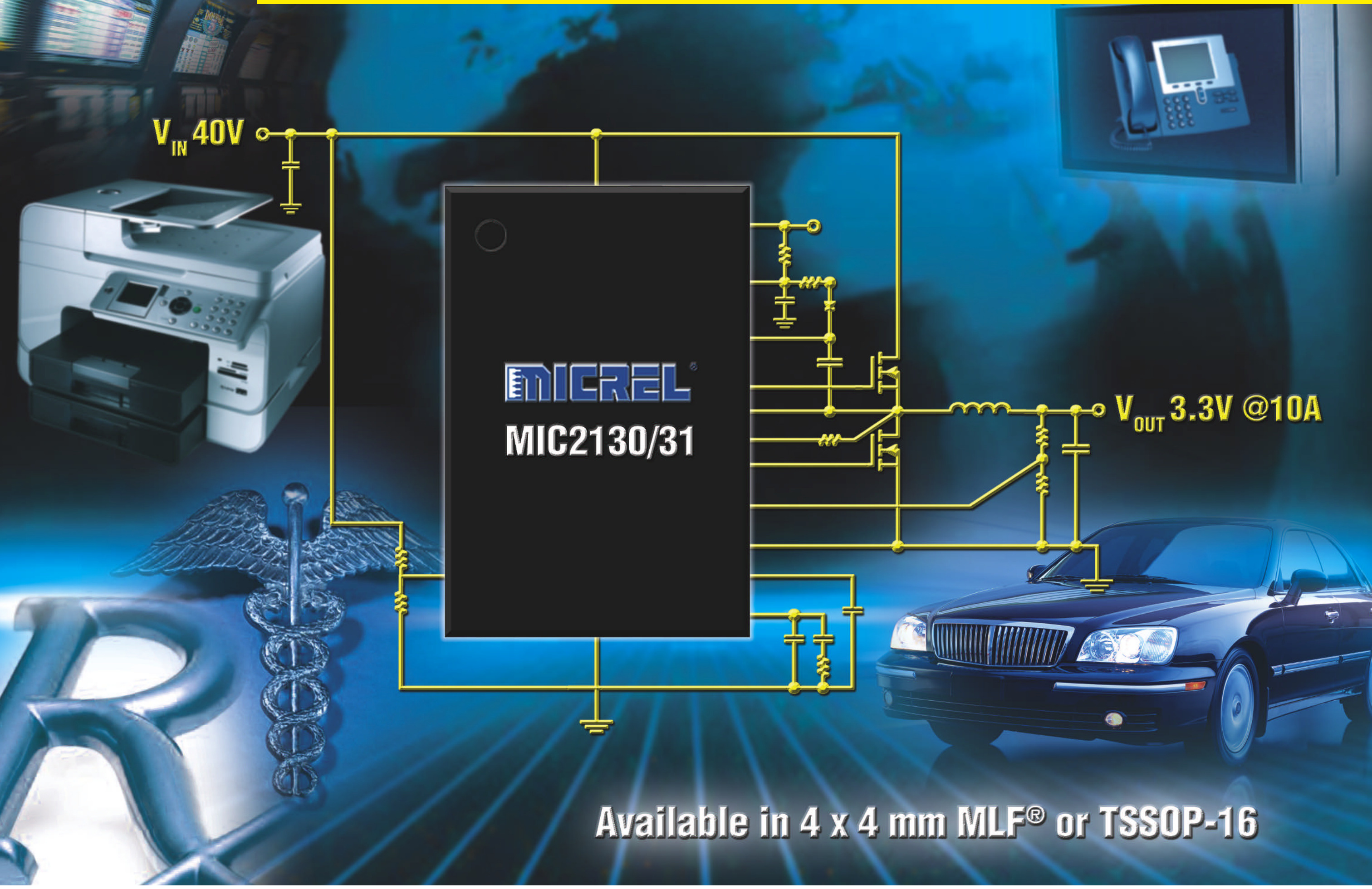
High-Voltage Synchronous Buck Control IC With Low EMI Option



Key Points:

- 8V to 40V input voltage range
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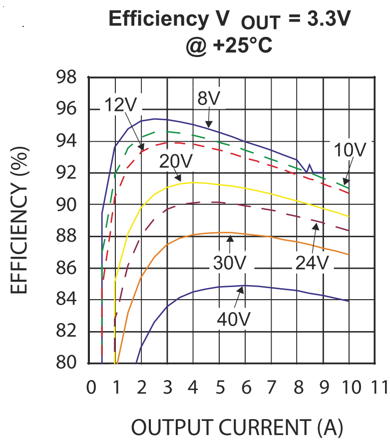
- Output over-voltage protection
- Tiny 16-pin 4mm x 4mm MLF® package option
- 16-pin e-TSSOP
- Junction temperature range of –40˚C to +125˚C

Applications:

- Automotive Systems
- Industrial/Medical DC-to-DC Point-of-Load
- Gaming Machines
- LCD/Plasma TVs
- Printer Head Drivers
- Telecom Systems



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EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS & INNOVATORS

Quad data converter features dual FPGAs

Targeting teams working on wideband-radar and -communication systems, Pentek recently released the Model 7150 high-speed data converter, featuring four 200-MHz, 16-bit ADCs and a pair of high-performance Xilinx (www.xilinx.com) Virtex-5 FPGAs. The 200-MHz sampling rate allows users to directly digitize nearly 100 MHz of bandwidth when the 7150 connects directly to the RF or the IF inputs of a communications system.

The single PMC (peripheral-component-interconnect-mezzanine-card)/XMC (express-mezzanine-card) module assigns strategic functions to both FPGAs for optimum performance. One targets interface connectivity, and the other performs real-time signal processing. The processing FPGA handles data flow and data routing, controls all clock and synchronization functions, and manages memory resources. The interface FPGA provides the board's system connectivity through a PCI-X or optional PCIe (PCI Express) interface.

The board's 1.5 Gbytes of synchronous DRAM supports real-time capture of 2.56 seconds of data sampled at 200 MHz. This large transient-capture capability is essential for applications such as wideband radar. You can synchronize multiple 7150s through a front-panel ribbon cable to create larger multichannel systems. The 7150 supports use with Linux, Windows, and VxWorks, and board-support packages for each operating system are available. Prices for the PMC version of the Model 7150 start at $13,500. The 135-MHz version of the 7150 is available, and the 200-MHz version will be available 14 to 16 weeks after receipt of order.

—by Warren Webb

▷**Pentek Inc**, www.pentek.com.

With four times the resolution and twice the memory of previous products, the model 7150 captures wide-bandwidth data with four 200-MHz, 16-bit ADCs.

IMEC LAUNCHES METHOD OF ANALYZING PROCESS VARIABILITY

To allow for optimization of system designs for timing, energy, and yield versus expected application load, the IMEC (Interuniversity Microelectronics Research Center) recently demonstrated a variability-aware-modeling flow that analyzes the process variability of smaller-than-45-nm technologies. The flow assesses the impact of process variations and degradation effects of these technologies on the system performance by giving valuable information to designers and can work with commercial DFM (design-for-manufacturing) tools. The research institution has validated the flow on industrial-process-technology data and IP (intellectual-property) cores.

The flow allows IP-block and system designers to assess their architecture-design options and to identify design bottlenecks before manufacturing to overcome functional problems and parametric uncertainty of designs that process and material variability of deep-submicron technologies cause.

According to Rudy Lauwereins, vice president of nomadic embedded systems at IMEC, until now, IDMs (integrated-device manufacturers) internally performed most variability-characterization work on their own technology and IP blocks. However, with the move to fabless companies, IMEC is attempting to bridge the gap between foundry and fabless companies on the design-level impact of using the most advanced semiconductor technologies. Qualcomm (www.qualcomm.com) and Samsung (www.samsung.com) are currently partners in IMEC's technology-aware design program.

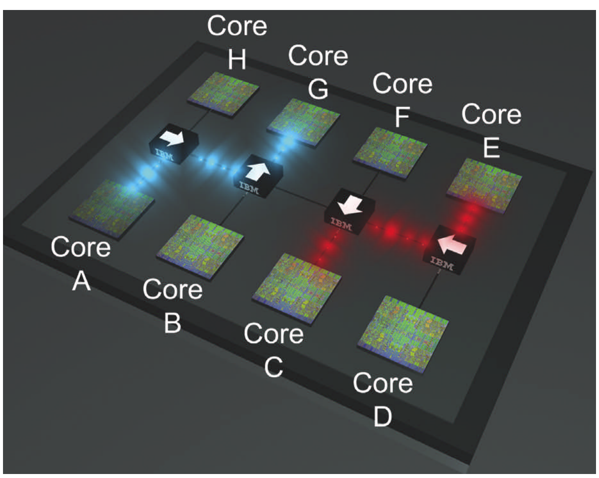
—by Ann Steffora Mutschler

▷**Interuniversity Microelectronics Center**, www.imec.be.

Tiny nanophotonic switch provides optical routing between cores

In another step toward sending information inside a computer chip using light pulses instead of electrons, researchers at IBM have created what they believe is the world's smallest nanophotonic switch, with a footprint approximately 100 times smaller than the cross section of a human hair. This development aims to address the trend within the microelectronics industry of increasing the parallelism in computation by multithreading, by building large-scale multichip systems, and by increasing the number of cores on a single chip, even though this approach makes sense only if each core can simultaneously receive and transmit large messages from all other cores on the chip, according to the company.

The cores on today's multicore microprocessors communicate with one another over millions of tiny copper wires, but this copper wiring would simply use up too much power and be unable to transmit the enormous amount of information for massive multicore processors. As such, IBM researchers are exploring an alternative by connecting cores using pulses of light in an on-chip optical network based on silicon-nanophotonic ICs. Like a long-haul fiber-optic network, such an on-chip network will transmit, receive, and route messages between cores that are encoded as pulses of light. The researchers envision that, using light instead of wires, as much as 100 times more information can travel between cores using 10 times less power and consequently generating less heat.



The silicon-broadband-optical switch (black boxes) performs the key role of directing traffic within the on-chip optical network.

This development is key to controlling the flow of information inside chips in the future and is expected to speed chip performance while using less energy. "This new development is a critical addition in the quest to build an on-chip optical network," says Yurii Vlasov, manager of silicon nanophotonics at IBM's TJ Watson Research Center. "In view of all the progress that this field has seen for the last few years, it looks [as though] our vision for on-chip optical networks is becoming more and more realistic."

In a paper published in the April 2008 issue of *Nature Photonics*, IBM details the development of a silicon-broadband-optical switch, which is another key component of on-chip optical interconnects. Once the electrical signals have changed into pulses of light, this switching device performs the key role of directing traffic within the network, en-

> This development aims to address the trend of increasing the parallelism in computation by building large-scale multichip systems.

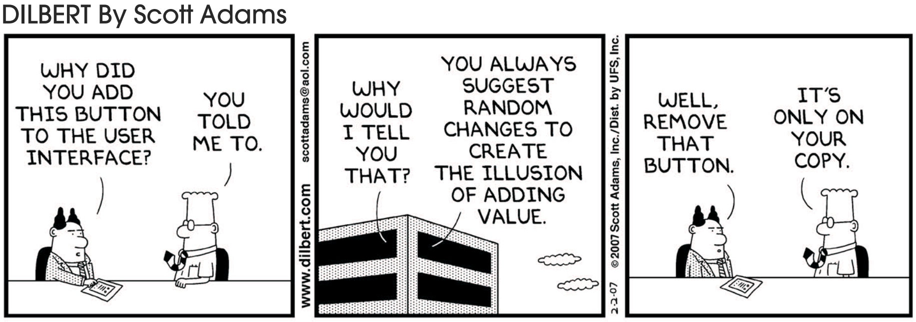
suring that optical messages from one processor core can efficiently get to any of the other cores on the chip.

The switch has several critical characteristics that make it suitable for on-chip applications. First, it is compact: As many as 2000 switches would fit side by side in 1 mm^2, thereby meeting integration requirements for future multicore processors. The device can also route a large amount of data because it can simultaneously switch many wavelengths of light. With each wavelength carrying data at speeds as high as 40 Gbps, it is possible to switch an aggregate bandwidth exceeding 1 Tbps, a requirement for routing large messages between distant cores.

Third, the researchers have showed for the first time that their optical switch can operate within a realistic on-chip environment, in which the temperature of the chip can change dramatically in the vicinity of hot spots, which move around depending upon the way the processors are functioning at any given moment. This temperature-drift-tolerant operation is a critical requirement for on-chip optical networks.

—by Ann Steffora Mutschler
▷**IBM Corp**, www.ibm.com.

DILBERT By Scott Adams



POE controller gears up for new physical layer

Anticipating the new 802.3at version of POE (power over Ethernet), Akros Silicon has introduced its AS1135 PD (powered-device)-controller IC, which the company claims is the first IC to implement the two-event PHY (physical-layer) classification of the IEEE 802.3at standard Draft 2.0. The new version of the standard raises the maximum available PD-controller-input power to 30W from the 13W that the 802.3af standard specifies. Some PDs currently offer 30W of power but use the handshake mechanism that the current standard specifies.

According to Amit Gattani, director of marketing for Akros, the draft version of the 802.3at standard states that an older device that cannot conform with the new classification scheme, relying instead on the older handshake sequence, receives only 13W of power, rather than 30W.

The AS1135 powered-device controller implements the two-event physical-layer classification function of the IEEE 802.3at standard Draft 2.0. This upcoming POE standard raises the maximum available PD-input power to 30W from the previously specified level of 13W that the 802.3af standard specifies.

The new 802.3at standard is under development, and the IEEE standards body has finalized the PHY classification, which allows PDs and PSE (power-sourcing equipment) to recognize each other as 802.3at-compliant. To implement the classification, the AS1135 provides the 802.3at-detection function on a logic-output pin, indicating successful POE connection to Type 2 PSE. The AS1135 can also operate with local-power input as low as 10V, so PDs and PSE devices integrating the AS1135 automatically adapt to legacy Ethernet and 30W 802.3at POE networks.

Ethernet systems are moving outside the more benign office or factory environment into regions such as China and India, which may have less stable power quality and in which lightning surges and noise can interfere with power and signal quality. As it did with its first POE product, the AS16XX, Akros continues with the AS1135 to emphasize on-chip EMI (electromagnetic-interference) filtering and surge suppression: The chip meets the IEC (International Electrotechnical Commission) 61000-4-2/3/4/5/6 and IEC 60950 requirements for surge protection, EMI filtering, and isolation. The chip is available in a 20-pin, 5×5-mm QFN with a ROHS (restriction-of-hazardous-substances)-compliant package and sells for $1.66 (1000).

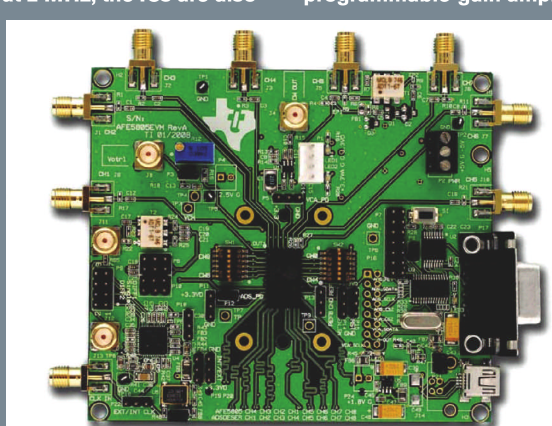
—by Margery Conner

▷**Akros Silicon**, www.akrossilicon.com.

LOW-POWER, LOW-NOISE ANALOG-FRONT-END IC TARGETS ULTRASOUND SYSTEMS

Texas Instruments' new family of analog-front-end ICs has power consumption of only 122 mW, making the devices suitable for portable-system applications. With noise performance of 0.85 nV/$\sqrt{Hz}$ at 2 MHz, the ICs are also applicable to high-channel-count, midrange-medical-ultrasound, sonar, and other applications.

The devices integrate eight channels of a low-noise amplifier; a voltage-controlled attenuator; a programmable-gain amplifier; a lowpass filter, and a 12-bit, 50M-sample/sec ADC with LVDS (low-voltage-differential-signaling)-data outputs.



The AFE5808 analog-front-end IC provides the key component of a medical-ultrasound system.

The resolution of a medical-ultrasound system depends on the number of channels it uses to acquire the information as well the noise level of those channels. A channel with lower noise allows better screen resolution. To save cost and power, portable ultrasound systems use 32 to 64 channels. High-end systems have 256 to 1024 channels. However, because of this device's low power consumption, you can use it in systems with high channel counts, such as the portable systems in ambulances. With these devices, emergency-medical technicians see high-resolution ultrasound images, which they can wirelessly beam to a hospital emergency room. Capturing a high-quality image in the ambulance saves valuable time if it obviates the need for performing a rescan of a patient on the hospital's high-end ultrasound machine.

The AFE5805 is available in a 15×9-mm, 135-pin BGA package with a suggested retail price of $75 (100). An evaluation module costs $199. Samples and evaluation modules are available now, and volume production is scheduled for June 2008.

—by Paul Rako

▶**Texas Instruments, www.ti.com/ultrasound.**

Multiprocessor system sports as many as four coherent, multithreaded cores

MIPS Technologies' multithreaded, multiprocessor, coherent-processing MIPS32 1004K licensable-IP (intellectual-property) platform supports as many as four single- or double-threaded processor cores that connect through a coherence manager. The nine-stage-pipeline architecture supports a worst-case 800-MHz-base-core operating frequency in a 65-nm TSMC (Taiwan Semiconductor Manufacturing Co, www.tsmc.com) general-purpose process.

The architecture implements a dual-core, dual-threaded configuration for a total of four threads. The architecture also has 32-kbyte caches for each core, a coherence manager, and a global-interrupt controller. The devices include 1004Kc integer and 1004Kf floating-point versions of the core, and they both support Revision 1 of the MIPS32 DSP ASE (application-specific extension).

The design-time configurability of the platform allows designers to size the instruction and data caches, TLBs (translation-look-aside buffers), scratchpad RAM, and user-defined instructions. The configuration must be the same for each core in a given implementation, however, so that the architecture can support SMP (symmetric-multiprocessing) operation with SMP-based operating systems.

The multicore coherence manager can manage one to four single- or dual-threaded cores, and it operates at the same clock rate as the cores.

The coherence manager supports cache-to-cache transfers, speculative reads to external memory, and global-cache operations. It manages coherency using the MESI (modified/exclusive/shared/invalid) protocol, and it employs redundant tags to enable L1-cache transfers and minimize the impact on processing performance. Designers control the coherence scheme with global-configuration registers.

> "The architecture implements a dual-core, dual-threaded configuration.

The platform supports an optional 256-bit interface that can manage fractional-clock-rate access to an L2 memory controller. The optional I/O-coherence unit bridges noncoherent I/O-peripheral data transfers so that the transactions are coherent within the system; it also supports per-transaction attributes for snooping L1 caches, L1 and L2 caches, noncoherent transactions, and I/O prioritization. The global-interrupt controller can route as many as 256 system-level and interprocessor interrupts to cores or VPEs (virtual-processing elements).

The SDE (software-development environment) for this platform includes the Gnu-based MIPS SDE-tool chain, the MIPSsim bus-functional modeling and instruction-set simulator, and the enhanced-JTAG and PDtrace system-navigator probe with coherence awareness. The two initial versions of this core, the integer 1004Kc and the floating-point 1004Kf, will be available for licensing during this quarter.

—by Robert Cravotta

▷**MIPS Technologies**, www.mips.com.

COMPACTPCI COMPUTER INTEGRATES MULTICORE TECHNOLOGY

04.17.08

A new 6U CompactPCI single-board computer from MEN Micro combines Intel's (www.intel.com) multicore technology with a flexible mezzanine-card extension to deliver the needed performance for a range of applications, including industrial automation, multimedia, aerospace, shipbuilding, medical engineering, and robotics. The D9 can integrate the Intel CoreT2 Duo, CoreT Duo, or Celeron M processors, depending on application requirements. The D9 offers a combination of I/O functions, including mezzanine-extension cards and XMC (express-mezzanine-card) or PMC (peripheral-component-interconnect-mezzanine-card) modules.

Two PCI Express links with one lane each control the XMC module, and the PMC module offers 32- or 64-bit performance and 33-, 66-, and 133-MHz speeds for PCI-X (PCI extended). Six USB 2.0 interfaces, as many as four UARTs, and as many as four Gigabit Ethernet ports are available at the front or the rear of the D9.

In addition, you can access PICMG (PCI Industrial Computer Manufacturers Group, www.picmg.org) 2.16 through a mezzanine card. The D9 also offers a CompactFlash slot and two SATA (serial-advanced-technology-attachment) ports that you can use onboard or on the backplane. The board operates in Windows and Linux environments as well as with real-time operating systems that support a multicore architecture. Prices for the D9 start at $3032.

—by Warren Webb

▶MEN Micro Inc, www.menmicro.com.

The D9 CompactPCI single-board computer offers multicore technology with a mezzanine-card extension for industrial applications.

VOICES

Freescale's Lisa Su: embedding future growth

Lisa Su, senior vice president and chief technology officer at Freescale Semiconductor (www.freescale.com), discusses the future of embedded-system technologies, differentiation beyond Moore's Law, and the challenges that come with an increasingly sophisticated electronics market. For more of this interview, visit www.edn.com/article/CA6541920.

What tech areas hold future growth for Freescale?

A Our core markets are in networking, automotive, and wireless. Those are large, good markets where we have good positions. We are starting to see … that the consumer market is a significant growth opportunity. The applications of some of the technology we have built for the networking and automotive [markets] are making their way into the consumer area, especially with multimedia. Our [goal] is to put embedded electronics in every application—the everywhere, every place, every time.

What challenges are you facing in achieving that goal?

A Probably the biggest challenge that I see for the industry is [that] electronics are getting more sophisticated. It's upon us as an industry to make [electronic devices] a lot simpler to use. It's great to have all this technology, but, if we can't get that [technology] into applications—if we can't get that hooked up and connected and working together—it's not as useful to the overall goals. We are spending a lot of time not just on the chip itself, but on the … package around the chip, so that we can get it quickly into new applications, particularly when you are doing things like making chips that will go into next-generation automotive electronics.

Automotive is a highly demanding and time-intensive market. How difficult is the automotive market to navigate from the technological and business standpoints?

A It is a challenging market from the standpoint that it takes a long time to design in. On the other hand, it is also an opportunity. … We can see that there will be a lot of growth. Even if the number of cars grows at a certain rate, the amount of electronics as a percentage of the car is going up. Probably the largest challenge is to ensure that the quality levels are where they need to be. There should be zero defects. We can't afford to have a quality incident.

Where do you see wireless technology going?

A Certainly, the adoption rates of 3G are there. There are a number of standards across the different geographies. Being able to keep pace with those standards is an important thing. The technology is going to be there. It's really the adoption rate of the infrastructure and ensuring that the competing standards get worked out.

How important is Linux to wireless growth?

A Linux is extremely important, *period*. It is a great opportunity to get application developers on a common operating system. It's important in both wireless and other consumer, multimedia applications.

What is Freescale's 'more than Moore' strategy?

A When you take a look at where you can differentiate in semiconductors, it used to be that scaling was king and companies would spend most of their time ensuring that you could get to smaller, faster, cheaper every two years. We are finding … that scaling is important; however, there are a lot of other ways to differentiate. It's about the software [and] the system that it comes in. Packaging is sometimes an afterthought, but I view it as a place [for] new opportunities to differentiate. 'More than Moore' for us means that we will continue pushing advanced technology from a scaling standpoint but that we are [also] looking for other ways to differentiate and make our products more valuable to the consumer.

What are Freescale's packaging-technology plans?

A As we make chips smaller and smaller, one of the issues is [the constraints of] the number of connections you need to make and the wire-bond pitches. So we developed … RCP [redistributed-chip packaging]. The idea … is to take some of the wafer-level elements, such as lithography and plating, and build wafer-scale packaging. [RCP is] one of our most innovative technologies, and it will reduce package sizes by 30%.

What is Freescale's networking road map?

A Multicores have been in PCs for a while, but they haven't broken into the embedded space in a big way. … You have this network infrastructure that is already in place, and you need to be able to migrate it to the higher performance, lower-power design points in a way that's really very easy to do. Our networking road map is aggressively going after multicore in 45-nm technology.

You seem to refuse to make a choice between being a researcher and being a businesswoman. How do you balance those two worlds?

A I believe that technology is really exciting but only when it gets out into the marketplace and when you can see it in a product and an application. The best technologists understand what's going on in the market and in the business environment. I happen to be chief technology officer of Freescale, but I'm very interested in ensuring that I understand personally what our customers are thinking and where the market is going. That's what will make us more successful.

—by Suzanne Deffree

RAQ's

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Contributing Writer John Ardizzoni is an Application Engineer at Analog Devices in the High Speed Linear group. John has been with Analog Devices since 2002, he received his BSEE from Merrimack College in N. Andover, MA and has over 28 years experience in the electronics industry.

Political Correctness and Datasheets

Q. Datasheet Specifications: Provoking or Confusing?

A. That's a matter of opinion. We receive many comments about our datasheets, mostly "good," "well done" or "reliable data." On some occasions, however, customers complain about missing information (usually specific to their application), or the occasional typo that finds its way into a datasheet. We're used to receiving a breadth of comments about our datasheets, but rarely do we get calls that are completely unexpected.

A recent call started well, with the caller, Ms. April Day, commenting that our products performed admirably, but she found our datasheets to be a little difficult to read. I chuckled to myself and told her, "Yes, some of our engineers can get carried away when writing datasheets." The conversation took a turn into uncharted territory when she said the datasheets weren't technically difficult to read, but that they were not "PC" friendly. I assured her that our datasheets could be viewed or printed from any computer. "No, no," she said, "I mean politically correct." She then proceeded to rattle off the offending aspects of the datasheet. When she had finished her list, my chin was severely bruised from having hit my desk top so often during her call.

She was quite enthusiastic and passionate about her cause, and I told her we would take her comments under advisement. After mulling over her comments with some of my colleagues, we came up with some creative "PC" alternatives that could be implemented into our datasheets. Following is her list of offensive parameters; with our "politically correct" alternatives in italics.

Input bias current… *Input non-discriminatory current*, Voltage Noise… *Silence Challenged Voltage*, Thermal resistance… *Non-receptive thermal conduction*, Common Mode Rejection Ratio… *Bourgeois Mode No-Dice Ratio*, *Disable pin… Differently abled pin*, Negative feedback… *Non-Positive feedback*, Absolute Maximum ratings… *Genuine Zenith ratings*, Power Supply Rejection Ratio… *Power Supply Refusal Ratio*, Negative power supply… *Unaffirmative power supply*, and Harmonic Distortion… *Spectral Purity Assessment*.

Ms. Day was quite pleased with our new phraseology and appreciated our quick response in resolving this issue. I told her that if one of our parts met with an early demise in her application, she could return it to our Analysis Laboratory for a complete *Deferred Success Analysis Report*.

By the way, I forgot to mention our caller's middle name… Fools, that's right April Fools Day. In case you haven't realized it yet, this RAQ has been an April Fools' Day[1] joke, rest assured we will not be incorporating any of these changes into our datasheets. See you next month!

[1] *April Fools' Day or All Fools' Day, is not an official holiday, but is celebrated in many countries on April 1st. The day is marked by playing practical jokes on family, friends, enemies and co-workers.*

To Learn More About Datasheets

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ANALOG DEVICES

BY BONNIE BAKER

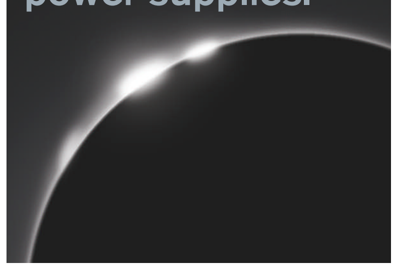
Does ENOB tell the whole story?

Near the beginning and end of a total solar eclipse, the thin slice of the sun that's visible appears broken up into beads of light. These lights are called Baily's Beads, after the British astronomer Francis Baily, who first noted the phenomenon in 1836 (**Reference 1**). At the moment they occur, you can't see the full picture; much more is going on. For a short time, you cannot see the sun. In same way, the ENOB (effective-number-of-bits) spec describes only part of an ADC: noise and distortion—rather than providing a precise or accurate description of an ADC.

Be aware of the ENOB pitfalls. It does not describe the converter's entire operation over the ranges of sampling frequencies and power supplies. Additionally, ENOB numbers exclude dc specifications, such as offset and gain error. Engineers use either an ac or a dc input signal to determine an ADC's ENOB. With an ac input signal, the digital output in an FFT (fast-Fourier-transform) plot shows the fundamental input signal along with the converter's noise and distortion. In the ac environment, you calculate ENOB from the converter's SINAD (signal, noise, and distortion), which is the same as THD+N (total harmonic distortion plus noise) or SNR+D (signal-to-noise ratio plus distortion). SINAD is the calculated combination of the SNR and the THD: $\text{SINAD (dB)} = -20\log_{10}\sqrt{10^{-\text{SNR}/10}+10^{+\text{THD}/10}}$.

THD combines all of the energy from the frequency bins in the FFT that are harmonic multiples of the input signal. To measure SNR, integrate all of the energy in the remaining bins and compare them with the fundamental signal level. Use the following calculation to derive ENOB from SINAD: $\text{ENOB}=(\text{SINAD}-1.76)/6.02$. In this simple formula, 6.02 is a multiplier of a 20 $\log_{10}$ of the converter's bits, and 1.76 is the quantization noise.

ENOB does not describe the converter's entire operation over the ranges of sampling frequencies and power supplies.



Using a dc input signal to measure ENOB involves the use of a histogram of the digital output. It shows the average dc value of the input signal and the internal noise of the converter. The most common measurement for oversampling or delta-sigma ADCs is to calculate the standard deviation, which is equal to the rms noise. If you apply a dc signal to a delta-sigma ADC and record a large number of samples, you can then derive the standard deviation for these codes. The formula for ENOB is: $N-\log2(\sigma)$, where σ is the standard deviation of data and N is the number of converter bits. With delta-sigma converters, ENOB, or the effective resolution, changes with adjustments to the oversampling or decimation ratio. Generally, the effective resolution of delta-sigma ADCs decreases with increasing data output rates.

ENOB for ac measurements uses a SINAD calculation, which is a combination of the SNR and THD. The ac measurement is dynamic, requiring a sine-wave input. You use this calculation with converter architectures, such as SAR (successive-approximation-register), pipeline, flash, and high-speed delta-sigma converters. ENOB for dc measurements uses rms, or the standard deviation of the noise calculation with a dc input signal. Slower delta-sigma converters use this type of measurement.

In both cases, remember that ENOB is a simple although somewhat superficial figure of merit, but it still has its place. So, when you use ENOB to make decisions, take time to look beyond the Baily's Beads in your eclipse. In some cases, the ENOB value may be misleading, when you may have a perfectly usable converter for your application. **EDN**

REFERENCE

1 "Baily's beads," http://en.wikipedia.org/wiki/Baily's_beads.

Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

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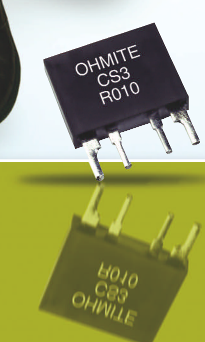

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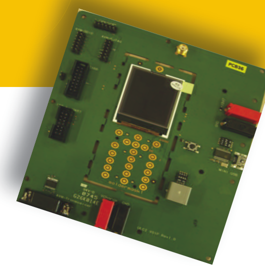
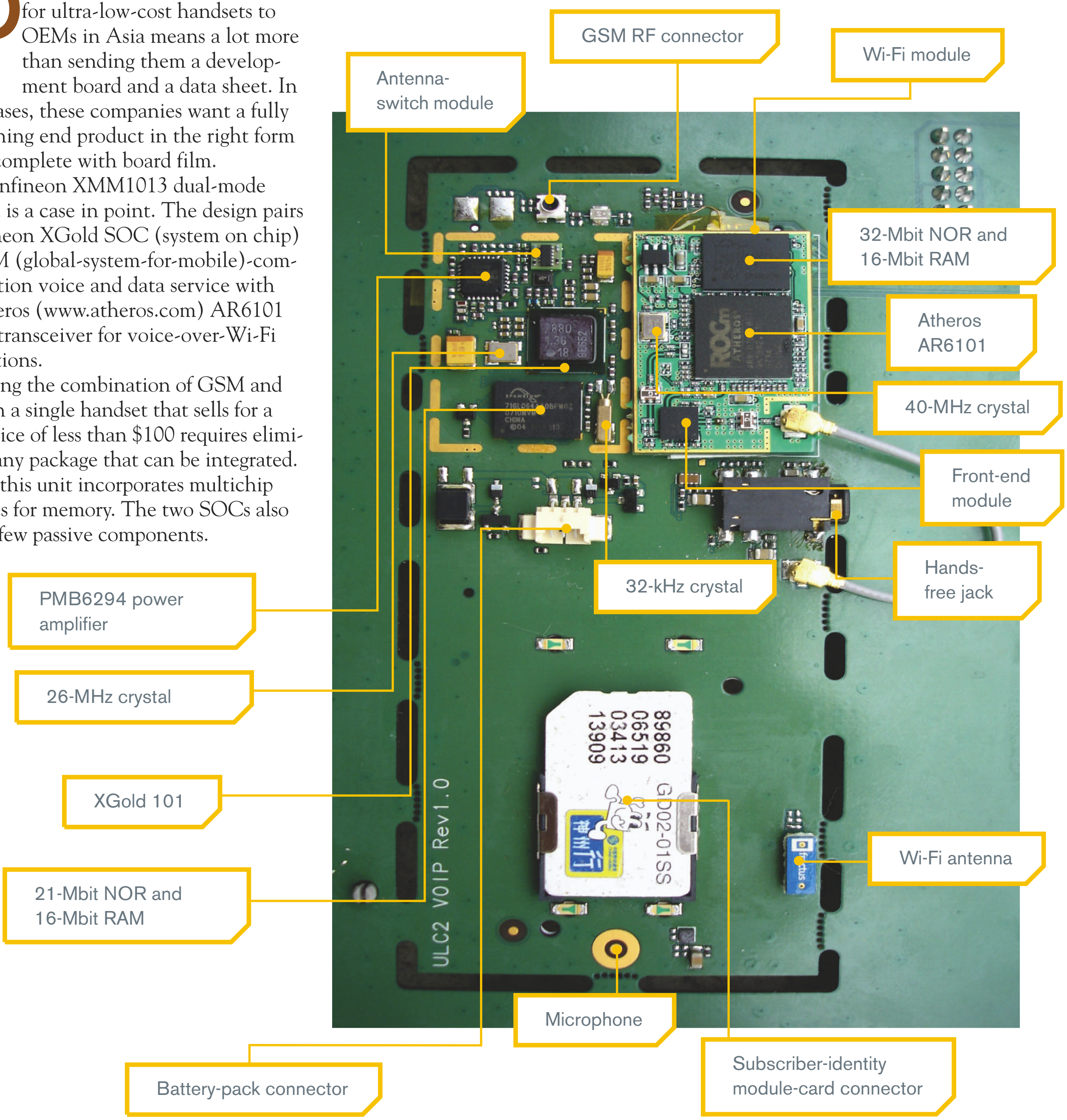


You can punch out and manufacture this cell-phone reference design

Providing a reference design for ultra-low-cost handsets to OEMs in Asia means a lot more than sending them a development board and a data sheet. In many cases, these companies want a fully functioning end product in the right form factor, complete with board film.

The Infineon XMM1013 dual-mode handset is a case in point. The design pairs an Infineon XGold SOC (system on chip) for GSM (global-system-for-mobile)-communication voice and data service with an Atheros (www.atheros.com) AR6101 802.11 transceiver for voice-over-Wi-Fi applications.

Keeping the combination of GSM and Wi-Fi in a single handset that sells for a retail price of less than $100 requires eliminating any package that can be integrated. Hence, this unit incorporates multichip packages for memory. The two SOCs also require few passive components.



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Basic DC Accuracy	250 ppm	35 ppm	30 ppm	30 ppm
Max Readings/s (continuous to PC)	19	1,000	10,000	50,000
Connectivity	USB	GPIB RS-232	GPIB, USB, LAN LXI Class C	GPIB, USB, LAN LXI Class C
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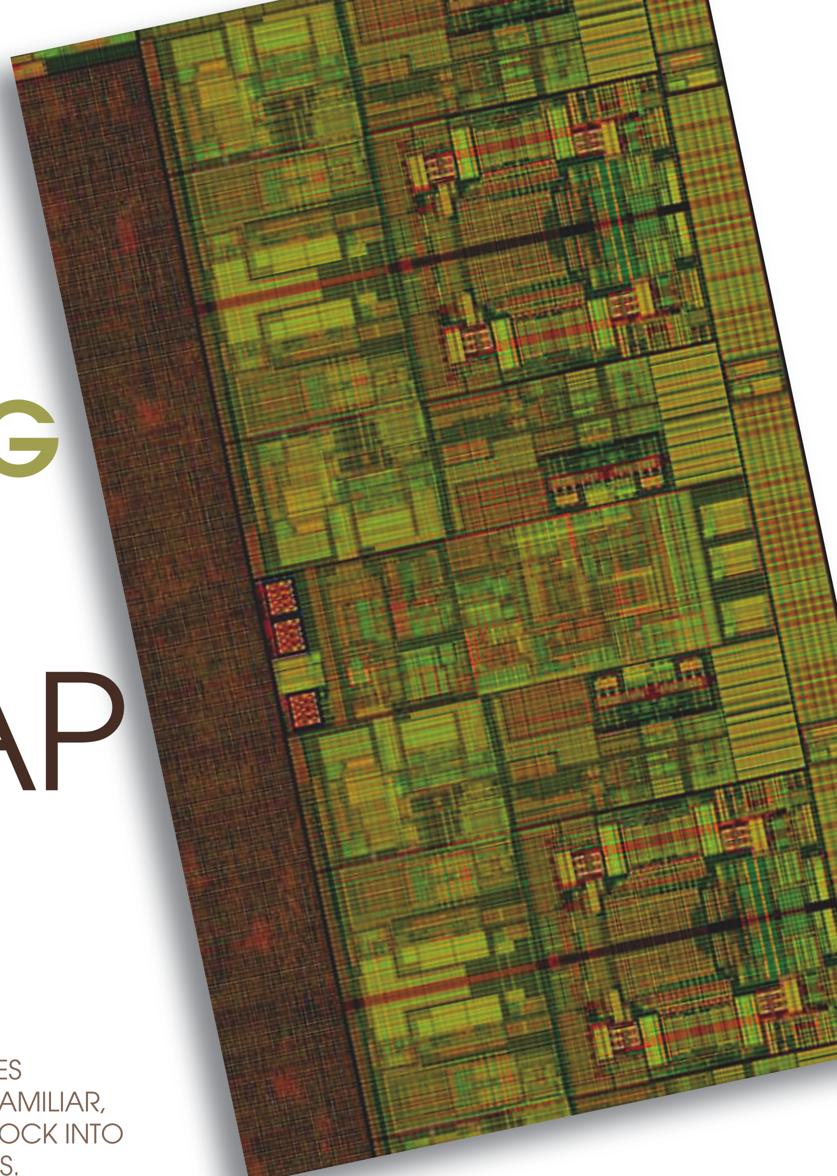

Figure 1 A serial interface block, such as this PCI Express PHY, can carry considerable complexity.

INTEGRATING HIGH-SPEED SERIAL I/O: NO SNAP FOR SOC DESIGNERS

BY RON WILSON • EXECUTIVE EDITOR

EXAMINE THE PROBLEMS AN SOC TEAM FACES IN INTEGRATING WHAT MANY SEE AS AN UNFAMILIAR, PARTICULARLY DELICATE MIXED-SIGNAL-IP BLOCK INTO THEIR ALREADY-CHALLENGING CHIP DESIGNS.

High-speed-serial-data transfer has ancient roots in the worlds of mass storage and communications. But increasingly, high-speed serial I/O is the method of choice for getting large amounts of data on and off SOCs (systems on chips). System designers are seeing high-speed serial I/O as an alternative to the wide parallel buses that were common on processor chips and SOCs.

"In our DSP space, high-speed serial started out as chip-to-chip interconnect and evolved into use in backplanes," says Ramesh Kumar, manager of wireless-baseband infrastructure at Texas Instruments. "In basestations, you have lots of data moving around. We saw buses go to 64 bits wide and then to 100 MHz, but this [increase] still wasn't enough to keep up with the data-flow needs.

"So, several generations ago, we offered high-speed-serial-I/O pins as alternatives alongside the wide buses. Initially, customers looked at the serial links and avoided them because of the apparent difficulties. But that [situation] has changed totally now."

A version of this evolution has taken place across the SOC industry, as fast data flows move from wide buses to RapidI/O, GbE (Gigabit Ethernet), HDMI (high-definition-multimedia interface), or some other serial standard. The change has the potential to vastly simplify board layout, substantially reduce the energy that data transfers consume within systems, and avoid signal-integrity nightmares. But it is not without challenges of its own for both chip and board designers.

WHAT'S INSIDE

Most often, SOC teams implement a high-speed serial link by licensing and integrating a piece of third-party IP (intellectual property). Even TI's baseband-chip teams, with their substantial resources, import serial-I/O IP from other teams within the company. Design teams with no high-speed serial-expertise must

AT A GLANCE

- Increasingly, SOCs (systems on chips) are using high-speed serial I/O for chip-to-chip interconnect.
- Most SOC teams use third-party IP (intellectual property) to implement the interfaces.
- Both selection and integration of high-speed serial interfaces are challenging.
- Success depends on the flexibility and robustness of the IP design.
- High-speed serial I/O is here to stay and probably to proliferate.

license third-party IP from outside, making it vital to understand the contents of a technological component such as a PCIe (peripheral-component-interconnect-express) or GbE I/O block.

The first thing to observe about a fast serial-I/O block is that it is not a trivial piece of silicon. For a technology such as PCIe, just the PHY (physical) interface can be large and complex, and it can be a significant power sink (**Figure 1**). The PHY layer typically contains a local oscillator, a phase-locked loop, and other CDR (clock-data-recovery) circuitry; handcrafted clock and power-distribution networks; and serial-to-parallel-conversion logic. The analog portions of this block operate at the full clock frequency of the data link, which can be 1 to 10 GHz. In addition to the PHY layer, there will normally be a mostly or all-digital-protocol-controller block, a mostly analog-I/O-transceiver block, and often a fourth block of supporting circuitry to provide supervisory functions ranging from power and clock gating, to digital-configuration logic, to a microprocessor interface. The two digital blocks may be synthesizable, but the two mixed-signal blocks are not.

The SERDES (serializer/deserializer) and its associated analog circuitry is normally hard IP. "In some ways, this [situation] makes integration of high-speed I/O simpler," observes Prasad Subramaniam, eSilicon's vice president of design technology. "You can apply pretty standard practices for shielding, isolation, and signal integrity and otherwise treat the analog block as a black box." Whether the I/O-transceiver cells are embedded in the SERDES or separate, you must treat them with care; they can be complex and are distinct from standard-library-I/O cells, but they are also hard IP.

The rest of the interface, including the protocol controller and most supporting circuitry, normally are synthesizable RTL. Thus, the complete package would comprise a few synthesizable pieces and one or more hard, process-specific blocks.

SELECTING A VENDOR

Like any other high-performance mixed-signal IP, high-speed serial-interface blocks require careful selection—perhaps more care in the choice of vendor than in the IP itself. Design managers and IP vendors alike say that the difficulty of integrating high-speed I/O blocks and the success rate both depend heavily on the IP vendor. "When you are talking about something like a PCIe [generation]-2 interface at 5 GHz, ... the IP is running very fast, [and] the receiver is operating on very small margins," observes Navraj Nandra, director of product marketing at Synopsys. "There are many other issues IP vendors must deal with, as well. They must have a deep understanding of signal-integrity issues and detailed knowledge of link termination for the interface in question. And these high-speed links have to be self-diagnostic: The IP must include sufficient design-for-test provisions."

Nandra warns that, even with a laundry list of skills to check off, vendor selection and evaluation of a piece of IP cannot be easy tasks. He divides his view of the evaluation process into three areas: For I/O that conforms to an industry standard, he recommends independent compliance testing of test silicon fabricated in the process you intend to use. Nandra emphasizes the importance of not inferring anything from a test chip that works at a different process node or even—when you reach more aggressive geometries—at a different process variant from the same node and foundry. The SERDES is a delicate RF design that porting can easily break.

Second, Nandra suggests getting a test chip in your process that contains both the interface IP and a programmable noise generator. "You want to get a characterization report that describes the IP's robustness in the presence of digital noise," he explains.

And, at 65 nm or smaller processes, Nandra says, you should see split-lot test chips in your process. "You need to

SIGNAL INTEGRITY FOR SOC DESIGNERS

By Lawrence Williams, PhD, Ansoft Corp

Gigabit-speed serial links move large quantities of digital data across today's telecommunication, high-definition video, gaming, and data-storage systems. SOC (system-on-chip) designers accomplish this data transfer by integrating specialized serial-I/O buffers to take advantage of modern serial interfaces, such as PCIe (peripheral-component-interconnect express), SATA (serial-advanced-technology attachment), GbE (gigabit Ethernet), and HDMI (high-definition-multimedia interface). Adopting these standards is now a requirement, but sending gigabit-speed signals from the IC die, into the package, and across a system PCB (printed-circuit board) can be a challenge.

Designers should be prepared to face: lowpass-filter design, handling differential signals, impedance matching from end to end of the serial link, driver rise-time issues, and modeling of the link as a complete system.

Designing SOCs with high-speed serial interfaces is a new challenge for design engineers. By adopting new strategies and tools, those engineers can explore high-density designs and accurately predict system performance.

AUTHOR'S BIOGRAPHY

Lawrence Williams, PhD, is director of business development at Ansoft Corp. Please go to www.edn.com/080417df1 for an expanded version of this sidebar.

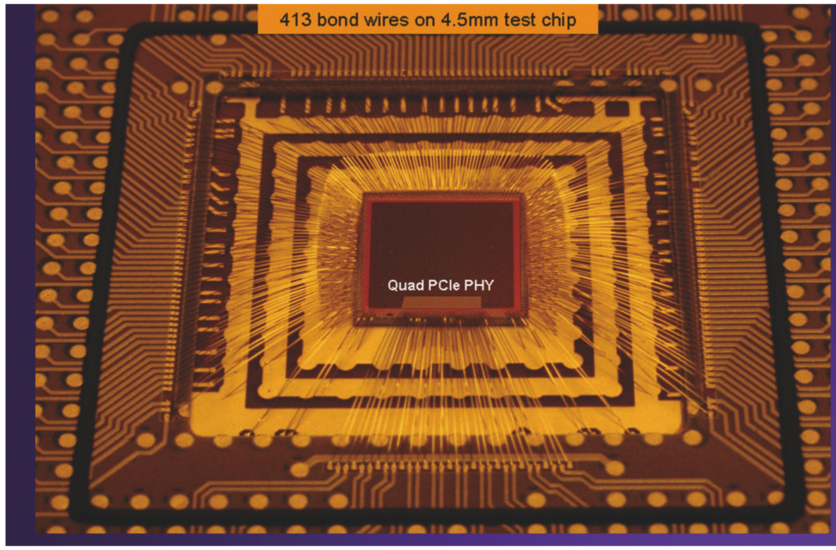

Figure 2 Test chips are useful in evaluating IP only if they allow for worst-case conditions, such as this Synopsys creation with remarkably long wire bonds.

understand your IP vendor's test-chip methodology," he says. "[The vendor] should be able to use the test chips to discuss with you the impact of process variations and voltage variations on the design, so you can address these variations in the layout." Nandra and others emphasize that the purpose of test chips is not to prove that the IP can work under some ideal set of conditions, but to explore its robustness across the whole range of conditions your design will encounter.

Hemant Shah, product-marketing director at Cadence, goes further. "The only way to feel good about your IP selection is to model the block in the board environment where the chip will be used." Shah warns that it does no one any good if the IP merely operates correctly on the die in loopback mode—it must exchange data with other chips across the board or backplane.

Therein lies a problem. Good tools exist for modeling the operation of high-speed-I/O pins with extracted board parameters, but the tools often lack good models. (See a condensed version of the **sidebar** "Signal integrity for SOC designers" on pg 32 and the full version at www.edn.com/080417df1.) "Vendors will often offer you IBIS [I/O-buffer-information-specification] models," says Subramaniam, "but they are minimally useful. Some IP vendors offer encrypted Spice models."

Those models help a little more, Subramaniam says, but they are still not enough to give you an idea of how a piece of serial-I/O IP will work with a package and board. For one thing, Spice's designers never intended it for this application and certainly not at these frequencies. For another, Shah points out, "Transistor-level models can be accurate, but, in practical terms, you can run them for only a few hundred bits of data transfer. That's nowhere near enough to get an idea of bit-error rate, which is a critical parameter."

Cadence has tried to attack this problem with an extension of the IBIS standard to provide for executable models that can accurately represent interfaces at these speeds. The company has proposed the extension to the IBIS committee, and Shah says that at least a couple of IP vendors are now shipping executable models they base on the proposal. But the idea still has a long way to go before achieving wide acceptance.

Another approach is to get S-parameter models of the package from the package vendor, and extract S parameters for the intended board design, and then hand this data back to the IP vendor and let the vendor characterize its own IP on its internal tools. That approach requires a certain amount of trust.

Subramaniam argues that the most practical approach is to get test silicon from the IP vendor—in your process—

put it into your package on your board, and measure it. Synopsys has tried to shorten this approach by providing test silicon in what it considers a worst-case wire-bond package (**Figure 2**) on the assumption that if the die works at the end of great loops of wire, it will work anywhere. "There's 5 nH on some of those wires," Nandra says.

IP INTEGRATION

Another important factor in IP-vendor selection is that your chosen vendor will be your partner during the integration process. And it will be a process.

"This is a critical mixed-signal-IP block," Nandra says. "You will want IP that is designed for worst-case placement on the floorplan. You will want documentation on the kind of guard rings, separate power supplies and grounds, and clock sources it will require. You will want rules and guidelines. Even so, support from the vendor is essential."

Subraminiam emphasizes that many SERDES designs require extremely clean clock signals. This situation probably holds truer with higher bandwidth interfaces. "Each SERDES design has its own requirements," he says. "Often, they require special, custom-designed clock-buffer cells in the clock-distribution network. These [cells] should come with the IP."

Routing becomes an exercise in signal-integrity analysis. "The big problems come when you are using multiple channels on one die," Subramaniam says. "You must do extensive simulation of the die/package/board combination. And placement, routing, and supply provisioning all become factors in signal integrity." Subramaniam says that eSilicon has developed its own simulation tool to deal with the problem.

As the integration process moves forward, dividing up the noise margin among the various sources becomes something of an art. Often, IP vendors give specifications on allowable supply noise. But they may not indicate how much margin their specification leaves for the rest of the system. If you use up too much with poor signal-integrity design on the die, you can have a surprise at the chip level. "You can end up needing a package that costs more than the die," Subramaniam warns.

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FLEXIBILITY IS A VIRTUE

All of this advice is great if you know in advance the details of the system environment. But more often, you don't know. What if you can't be sure about the package type or the board design? Programmability comes in handy in this scenario.

The I/O buffers on many high-speed serial blocks provide programmable pre-emphasis on the transmitter side and equalization on the receiver side, so the block can adjust to a range of environments. Perhaps the worst-case scenario for programmability would be FPGAs with on-chip serial interfaces. A single design must handle a small range of packages, a large range of interface stan-

dards, and a huge range of application scenarios.

Altera's design team focuses on these conditions. "We've found that it's easy to make a transceiver that mostly works," says Misha Burich, senior vice president for R&D. "But what you need is a robust design that leaves the margin to the customers rather than using it up internally." To cover the range of applications, Altera designs its own I/O cells with programmable pre-emphasis and adaptive equalization. "It's very special technology compared to our general-purpose I/O cells," Burich says. The Altera team also makes huge investments in modeling, simulation, and test chips. "We typically have two iterations of test chips for the I/Os," Burich says.

So, you spend a lot of time evaluating IP vendors, verifying that real test silicon works in your environment, and then working with the vendor to integrate the blocks following all the integration guidelines. At that point, what are your chances of success?

"If this is your first silicon at a new node, with proven IP, you have a good chance of success," says Subramaniam, "but not 100%. Not every design will be production-worthy on the first try, irrespective of the history of the IP."

For that reason, Subramaniam recommends an additional step: evaluating the IP not just to fit your application and its production history, but for its flexibility. "Look for a high level of software programmability. Look for good access for test and debug, and the ability to change all the settings on the critical circuits," he says. "To some extent, the more you can adjust things, the more you can avoid repair. And, just in case, look at the IP's internal routing to see how much the design can be altered with changes to just one or two mask layers."

For many SOC designers, high-speed-serial I/O is here to stay and probably to proliferate around the periphery of their die. Understanding the risks, the integration problems, and the flexibility that the chip user will need to meet package-cost goals and adapt to the board design is vital. Awareness of these factors is not only essential to design, but also necessary to properly evaluate the IP during the selection process. Even so, the most important steps may be measuring test chips in a realistic environment and making the IP work in an unanticipated environment. It's an uncertain art, but it is an art, not just a gamble. EDN

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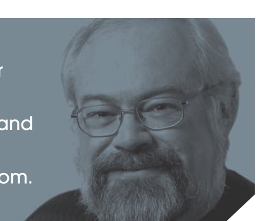


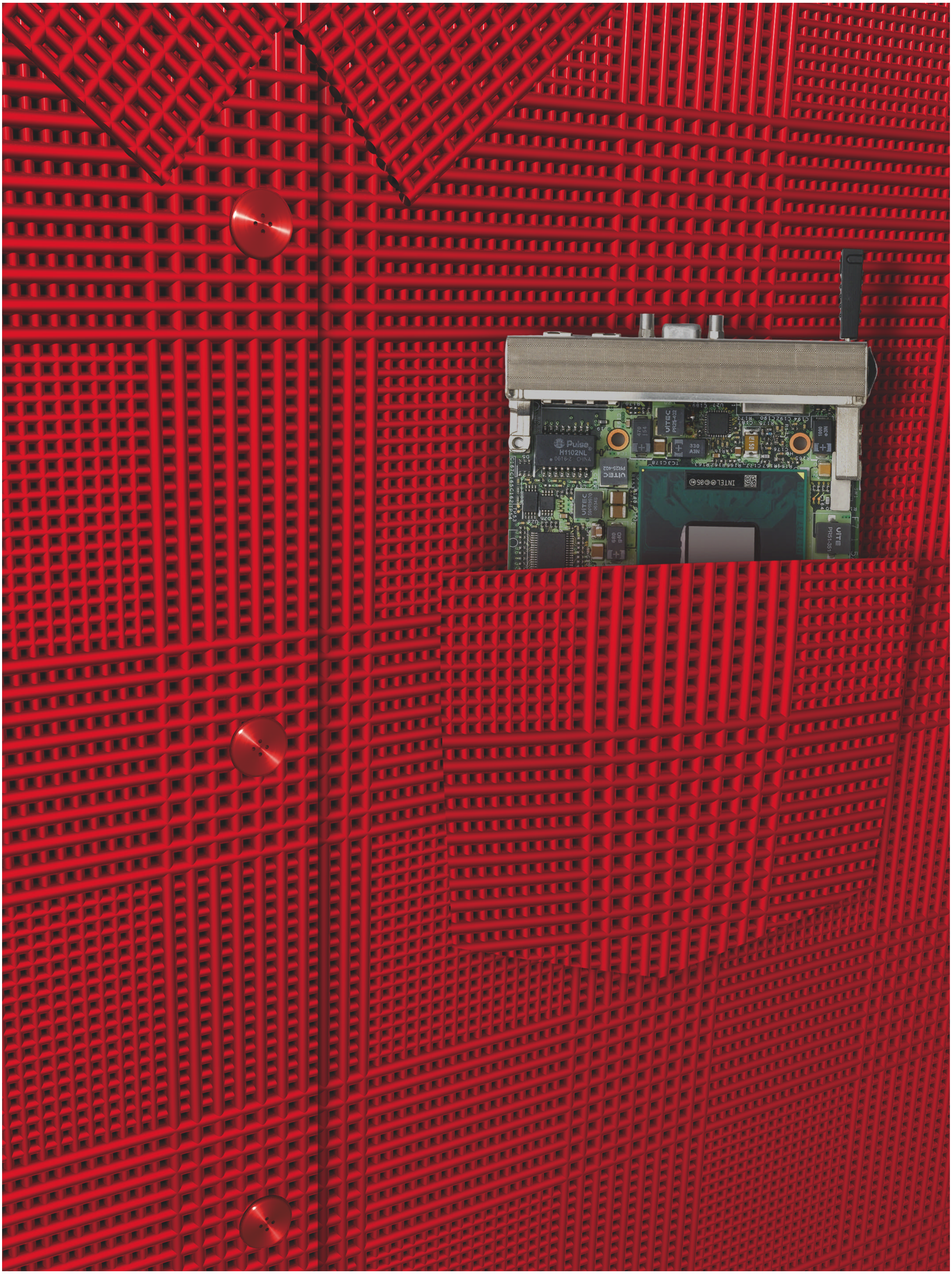
BY WARREN WEBB • TECHNICAL EDITOR

EMBEDDED TECHNOLOGY

DESIGNERS CHOOSE FROM THE LATEST FABRICS

As high-performance embedded systems stretch the limits of technology, board-level interconnection strategies require constant updating to match soaring data-transfer requirements. Designers can choose from a series of evolving and sometimes competing fabric-technology standards to extend system performance and preserve budget constraints. Medical instrumentation, military systems, communications installations, and process automation are just a few areas in which rising bandwidth, increased processing requirements, and escalating application complexity continue to expand the fabric-technology envelope.

EMBEDDED-SYSTEM DESIGNERS ARE USING THE LATEST SWITCHED-FABRIC TECHNOLOGY TO NOT ONLY BOOST DATA RATES, BUT ALSO DYNAMICALLY OPTIMIZE PERFORMANCE, BYPASS FAILED SUBSYSTEMS, AND COEXIST WITH LEGACY COMPONENTS.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New embedded designs traditionally rely on COTS (commercial off-the-shelf) processor and peripheral modules from the embedded-computing marketplace to reduce costs and shorten development schedules. Board standards eliminate the trial-and-error design iterations necessary to get optimal cooling performance and mechanical alignment. Standards-based designs also shorten the software-development effort by providing access to compatible operating systems, vendor-supplied drivers, and sample firmware. Most of the widely used embedded-board standards, such as PCI (peripheral-component interconnect), VME (Versa-module Eurocard), CompactPCI, and ATCA (Advanced Telecom Computing Architecture) already have several fabric-interconnection options so that designers can choose to bypass the shared-bus architecture where needed. However, as high-performance-embedded-system requirements stretch the limits of technology, standards bodies and COTS manufacturers are struggling to deliver a steady stream of updated products to meet the needs of a growing list of advanced applications.

Switched-fabric architectures allow datapaths between computing nodes to change dynamically to support multiple simultaneous data transfers. Designers use the term "fabric" to represent this architecture, because you can connect any node to any other node through datapaths that resemble the interwoven threads in cloth material. A major benefit of a switched fabric is that each connection is a direct point-to-point data path. This feature yields better electrical characteristics, allowing higher fre-

AT A GLANCE

- With high-speed fabric technology extensions, off-the-shelf shared-bus architectures continue to support today's high-performance embedded systems.
- Low-voltage swings and point-to-point transmission paths allow serial switched-fabric systems to extend data rates into the multigigabit range.
- Switched-fabric architectures can adapt to system failures by routing data around defective paths or processing modules while repairs are made.
- Multiple serial-fabric communications options in board-level specifications may lead to industry fragmentation and product-interoperability issues.

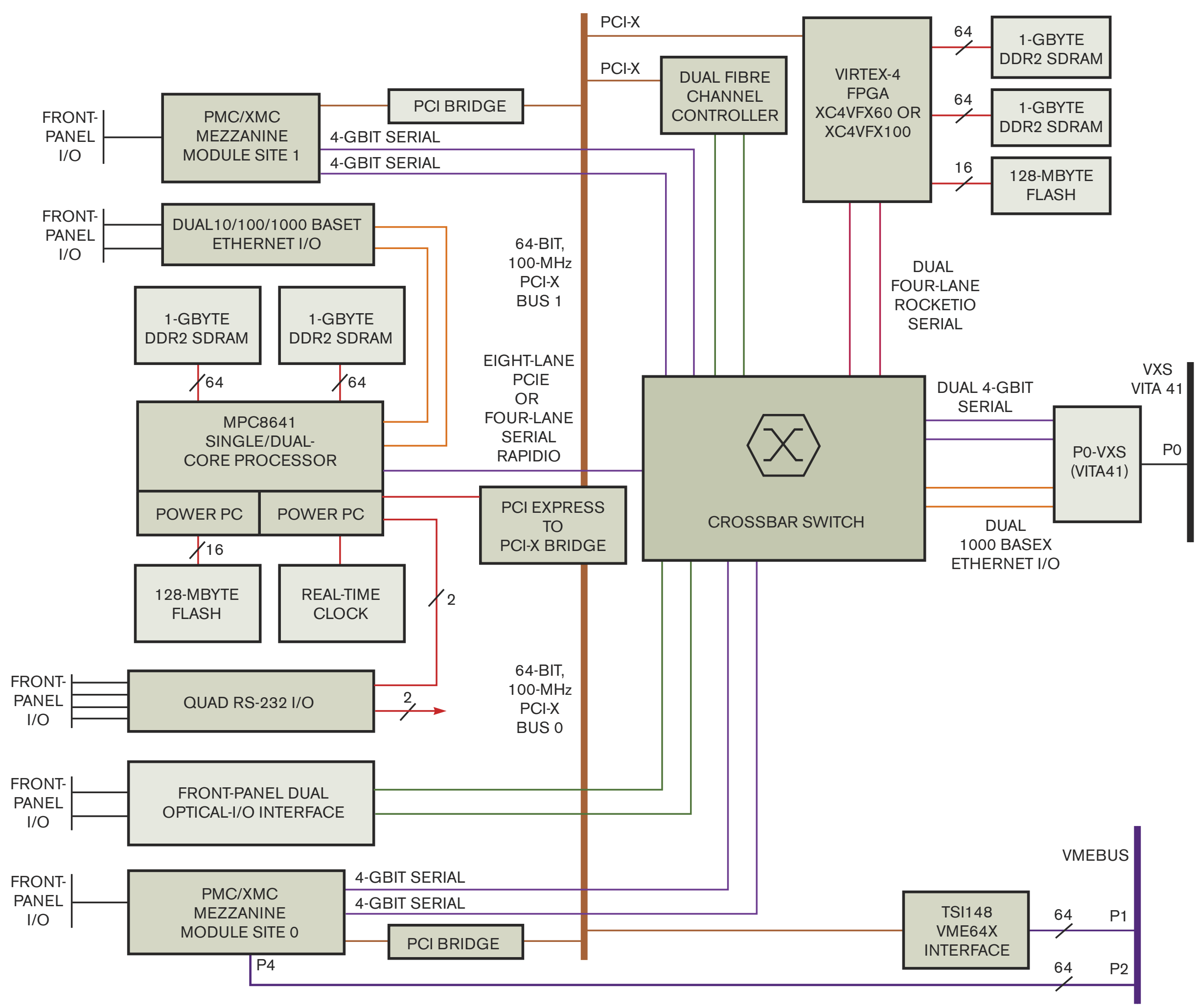

Figure 1 The Pentek Model 4207 VME/VXS digital-signal-processing and data-acquisition board features a fabric-transparent crossbar switch and multiple gigabit serial resources.

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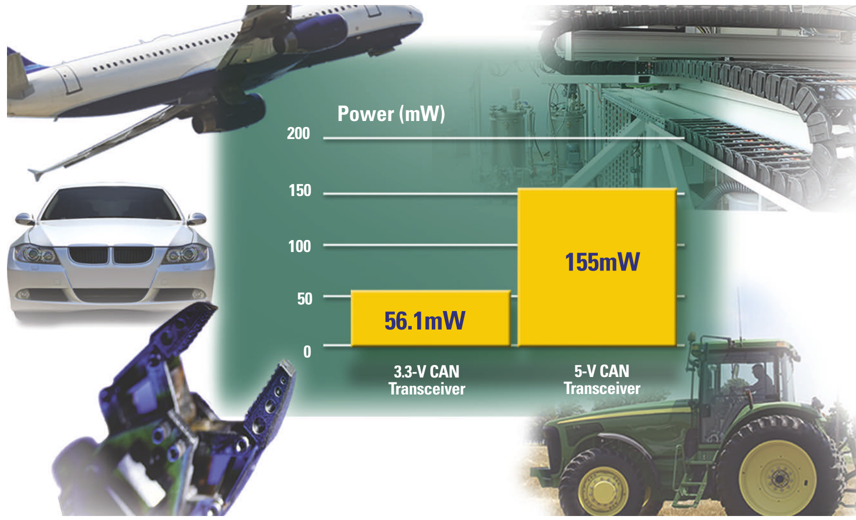

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quencies and bandwidth than bus architectures. A typical switching fabric uses multiple stages of switches to route transactions between a source and a target.

DIFFERENTIAL SPEED

Most of the switched-fabric specifications call for LVDS (low-voltage differential signaling) for maximum bandwidth between nodes. LVDS uses voltage swings of approximately 350 mV to communicate over PCB (printed-circuit-board) traces or a balanced transmission cable at thousands of megabits per second. With this much bandwidth, most systems use few parallel lines, opting instead for serial-data streams. This approach leaves plenty of room for future performance enhancements by simply adding parallel datapaths. Low-voltage swings and constant-current-line drivers deliver low-noise signals at low power consumption. The ANSI (American National Standards Institute)/TIA (Telecommunications Industrial Association)/EIA (Electrical Industries Association)-644, and IEEE 1596.3 specifications detail LVDS.

In addition to higher data rates, switched fabrics offer designers several system advantages. A major benefit is that each connection is a direct point-to-point datapath, thereby eliminating the multiple connections of a parallel-bus structure. Another obvious benefit of serial connections is the reduced connector sizes due to fewer signal lines. An integrated switched-fabric interconnection can also dynamically increase system availability by routing critical data around defective paths or nodes. Multistage switching allows the designer to easily scale interconnections as requirements change. You can install new switch elements along with new I/O components so that the system retains its interconnection flexibility as the system grows.

Product compatibility is one of the most complicated issues when upgrading or extending the performance level of board standards. VME and PCI have undergone multiple upgrades to increase the shared-bus data-transfer rate and allow legacy products to communicate at their original speed. Switched-fabric upgrades send high-speed data across the backplane through edge-card connections that are unused in the shared-bus configuration. Long-term availability is a prime requirement for many high-performance embedded products. Although the average life of desktop components is about 18 months, users expect typical embedded products to remain in service for five years or more. Some military projects ask for a 15-year life cycle.

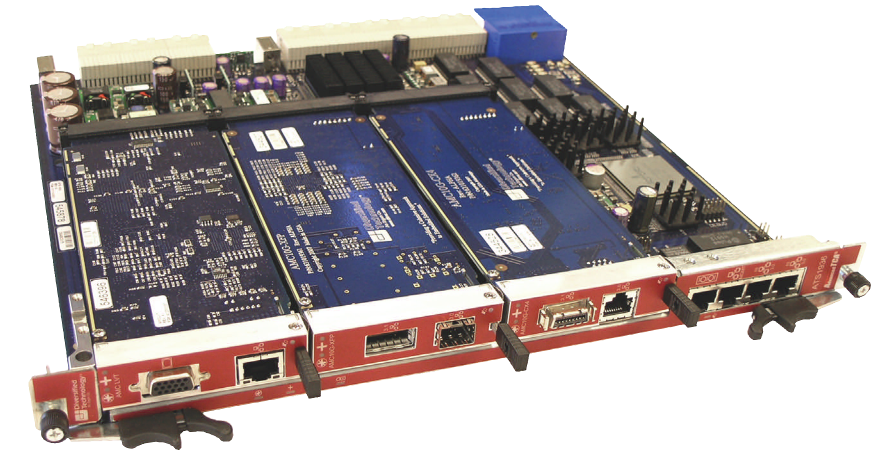

Figure 2 The ATS1936 ATCA Switch Blade features separate base and fabric gigabit-GbE networks plus three onboard AdvancedMC module sites.

PCIe (PCI Express) is one of the more popular fabric extensions and sees wide use in commercial desktop computers in addition to embedded designs. The basic PCIe link consists of two signal paths that use LVDS swings and constant-current-line drivers to communicate at 2.5 GT (gigatransfers)/sec in each direction. Standards bodies have approved Version 2.0 of the PCIe to increase this data rate to 5 GT/sec. However, because of the 8B/10B encoding scheme used to increase the number of transitions, the maximum effective data rate is 4 Gbps. You can easily increase the bandwidth of a PCIe link by simply adding signal pairs, or lanes, until you reach the desired performance level. The PCIe specification supports one-, two-, four-, eight-, 16-, and 32-lane widths. In August 2007, the PCI-SIG (special-interest-group) announced that the next version of PCIe will support a bit rate of 8 GT/sec.

INFINIBAND HAS BECOME THE FABRIC OF CHOICE FOR MANY HIGH-PERFORMANCE COMPUTING APPLICATIONS.

RAPID RESULTS

RapidIO, which the RapidIO Trade Association defines, is also a popular point-to-point interconnect technology. Originally conceived by Motorola and Mercury Computer Systems, the RapidIO packet-switched architecture transmits data and control information between computing and peripheral nodes in embedded systems. Full-duplex point-to-point links have one or four high-speed serial lanes and 8B/10B-encoded data transmission at signaling rates of 1.25, 2.50, or 3.125 Gbaud for peak bandwidth of 20 Gbps. The association based the initial RapidIO specifications on bit-parallel clock and data, but subsequent specifications have adopted serialized-clock and -data transmission to reduce pin requirements and extend signal reach.

InfiniBand, another popular high-speed interconnect, has become the fabric of choice for many high-performance computing applications. Like the channel model that most mainframe computers use, all InfiniBand transmissions begin or end at a channel adapter. Each processor contains a host channel adapter, and each peripheral has a target channel adapter. These adapters can also exchange information for security or quality of service. InfiniBand uses the 128-bit Internet Protocol Version 6 to uniquely identify each node and provide Internet compatibility. InfiniBand transmissions are either packet- or connection-based to support blocks or continu-

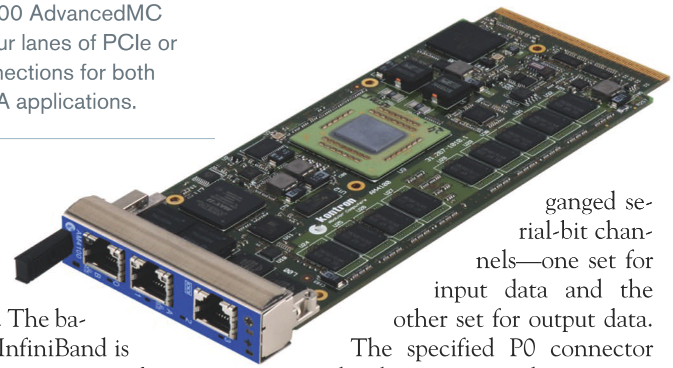

Figure 3 The AM4100 AdvancedMC module supports four lanes of PCIe or RapidIO fabric connections for both ATCA and MicroTCA applications.

ous streams of data. The basic technology for InfiniBand is a bidirectional link consisting of two LVDS pairs, providing one transmitting and one receiving path, each operating at 2.5 Gbps. A usable bandwidth of 80% of the signal rate yields a 2-Gbps or a 250-Mbps data rate in each direction. Higher bandwidth connections are possible by grouping four or 12 links for each transmission path. With 12 links, the effective throughput is 48 Gbps.

PCIe, RapidIO, and InfiniBand are among a number of similar fabric architectures now integrated into and spreading throughout standards-based, high-performance-embedded-system products. For example, CompactPCI, the rugged-form-factor equivalent of low-cost PCI-based desktop hardware, now defines serial-fabric interconnections with a series of optional addenda to the original specification. CompactPCI boards are based on the Eurocard industry standard defining both 3U and 6U board sizes and allow for front-loading and removal from a card cage. The more popular 6U version has as many as five connectors on the rear of the card, allocating two for the traditional CompactPCI bus; the remaining three connectors provide additional pins suitable for optional connections to backplane fabrics. CompactPCI and CompactPCI Express are open specifications that the PICMG (PCI Industrial Computer Manufacturers Group) supports and controls.

Similarly, The VITA (VMEbus International Trade Association) 41 VXS (switched serial extensions) append fabric technology to the venerable VMEbus standard and preserve product compatibility. The VXS specification defines a payload card, a switch card, and a new high-bandwidth P0-backplane connector and retains the standard P1 and P2 parallel VMEbus connectors. Each P0 fabric port consists of two sets of four ganged serial-bit channels—one set for input data and the other set for output data. The specified P0 connector technology supports data rates as fast as 10 Gbps for each serial channel. Payload cards are simply standard VMEbus processor, memory, or I/O boards with the addition of the new VXS-fabric interface. With no P1 and P2 connectors, switch cards have the same form factor as payload cards and include as many as 18 full-duplex serial connectors plus a power connector. The switch card contains the fabric switching necessary to route serial data between payload cards. To remain fabric-agnostic, VITA 41 subspecifications define switch and payload-card definitions for InfiniBand, serial RapidIO, GbE, and PCIe.

ONE SIZE FITS ALL

Pentek recently released its Model 4207 digital-signal-processing and data-acquisition system, featuring multiple high-speed serial interfaces in a VXS form factor (**Figure 1**). This new board employs Freescale's MPC8641D dual-core PowerPC AltiVec processor and a Xilinx Virtex-4 FX series FPGA. In addition, a fabric-transparent crossbar switch bridges multiple gigabit-serial resources, including the PowerPC and FPGA, two XMCs (express mezzanine cards), dual VXS ports, dual Fibre Channel ports, and two optical serial transceivers. The Model 4207 combines many standard interfaces and protocols including VXS, PMC (PCI mezzanine card), XMC, PCI-X (PCI extended), PCIe, GbE, RocketIO, RapidIO, Fibre Channel, Xilinx Aurora, and VME64x technologies, all of which the crossbar switch accommodates. Developers can take advantage of unused FPGA resources to implement custom signal-processing algorithms and to process captured data in real time. Prices for the immediately available Pentek Model 4207 start at $14,725.

With a larger form factor, high-availability features, and high-speed fabric interconnections, the ATCA provides a viable off-the-shelf alternative to the proprietary equipment common in the telecom industry. The ATCA specification provides hot-swap capability for all boards and active modules, allowing systems to achieve and even exceed the elusive "five-nines," or 99.999%, availability. The fabric interface provides a full-mesh interconnection in which each slot has a direct connection to every other slot. Because it has a built-in fabric interface, ATCA lacks the legacy-compatibility problems of other board standards. However, the basic ATCA specification does not call out a specific fabric technology for data transport. Instead, a series of subsidiary specifications define backplane details for the various fabrics, such as Ethernet, Fibre Channel, InfiniBand, StarFabric, PCIe, and RapidIO. Although this approach allows designers to build conforming boards with any fabric technology, it creates interoperability issues and promises to fragment the specifications.

Due to ATCA's telecommunications focus, GbE is the fabric of choice for many system designs, and the ATS1936 Switch Blade from Diversified Technology is a good example (**Figure 2**). The ATS1936 is a relatively low-cost ATCA switch complying with the core PICMG 3.0 ATCA specification plus the 3.1 Ethernet-fabric option. The blade features three AdvancedMC (advanced-mezzanine-card) sites for operations, administration, and management; firewall; and encryption applications. By separating the base and fabric networks, the ATS1936 provides a separate control plane and data plane and provides 1-Gbit Ethernet switching on the base fabric; the expansion paths provide 1- or 10-Gbit Ethernet switching. The single-piece price for the ATS1936 is $5245.

MEZZANINE FABRICS

To match the bandwidth and performance of the baseboard, AdvancedTCA designers added replaceable plug-in modules with many of the same features as the basic architecture. The resulting AdvancedMC standard offers designers a hot-swappable, field-replaceable module to lower maintenance costs and reduce downtime. AdvancedMC modules feature remote management and switched-fabric technology in an approximately 3×7-in. form factor. Modules come in single- or double-size configurations with compact, midsize, and full-size faceplates. On the interconnect side, AdvancedMC supports high-speed serial interconnects eventually to include all of the switched fabrics that ATCA allows. The basic specification defines a fabric interface with as many as 21 ports or 42 differential pairs, providing full-duplex, point-to-point connectivity between modules or to the baseboard. Rated at 12.5 Gbps per port, AdvancedMC can handle multiple lanes of the modern protocols such as Ethernet, PCIe, RapidI/O, and InfiniBand. Subsidiary specifications map the ports to specific fabric requirements.

With all the high-power, hot-swap, switched-fabric, and management features of AdvancedMC, designers devised a standard to use these modules to plug directly into a backplane for small, stand-alone systems. The standard, MicroTCA, provides a stand-alone chassis with a backplane that directly accepts AdvancedMC cards, thereby eliminating the ATCA carrier board. The MicroTCA specification defines a minimum system as a collection of interconnected elements consisting of at least one AdvancedMC module, a carrier hub, and a power module, as well as the interconnect, cooling, and mechanical resources to support them. The carrier hub combines the control and management infrastructure and the interconnect-fabric resources to support as many as 12 AdvancedMC modules. The smaller form factor makes the MicroTCA concept viable for lower budget applications in telecom and a range of embedded projects.

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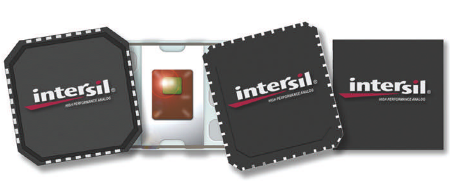

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Supporting both ATCA plug-in and MicroTCA applications, Kontron offers the AM4100 AdvancedMC module, which the Freescale MPC8641D 1.5-GHz, dual-core PowerPC processor powers (**Figure 3**). The module delivers as much as 2.3-MIPS computing performance, and its 4-Gbit-Ethernet interfaces support real-time-transmission protocol, checksum, quality-of-service, and packet-manipulation activities. The AM4100 includes as much as 2 Gbytes of soldered DDR2-SDRAM, 4 Mbytes of bootable NOR flash, as much as 4 Gbytes of NAND flash, and EEPROM for user and configuration data. Two of the 4-Gbit interfaces are routable to either the module-card-edge connector or the RJ45 connectors on the front panel. Additionally, the board supports four-lane PCI Express or serial RapidIO for high-speed fabric connectivity. The AM4100 is fully hot-swappable, which makes it possible to replace the module without shutting down the ATCA carrier board or the MicroTCA system. A dedicated module-management controller manages the board and supports ATCA-management-interface commands, which allow operators to more quickly detect and eliminate faults at the module level. AM4100 board-support packages are available for Linux and WindRiver's VxWorks operating systems.

Although several architectures still compete for the universal interconnect technology, there is little doubt that switched fabric has become a necessary part of most high-performance embedded systems. Current fabric systems have improved to the point at which additional gains bump into the physical limits of voltage-slew rates, connector characteristics, and transmission-path limitations. Therefore, the addition of parallel lanes will lead to most of the data-rate improvements in the future. As serial-fabric technologies become the limiting factor to system performance, designers will head to the laboratory and come through with the next-generation high-speed data-delivery system. Are we ready for optical paths? EDN

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BY EUGENE CABANBAN • PLX TECHNOLOGY

Blind prefetching improves PCI Express-to-PCI-bridge performance

STANDARD BRIDGES ALLOW DESIGNERS TO COMBINE THE HIGH-PERFORMANCE PCI EXPRESS INTERCONNECT WITH LEGACY PCI-BUS ARCHITECTURE. ADVANCED BRIDGE FEATURES, SUCH AS BLIND PREFETCHING, BOOST DATA THROUGHPUT.

New high-performance bridging devices, available from a number of vendors, enable designers to migrate legacy PCI-bus designs to the advanced PCIe (Peripheral Component Interconnect Express) serial architecture. These bridges reduce the time it takes for data to pass through the system, thus minimizing clock-hogging latency. However, many of these bridges provide an additional function that further maximizes throughput: blind prefetching.

Blind prefetching allows the bridge to read a predefined amount of data, in sequential addresses, from PCIe memory and to buffer the data in the bridge whenever a device on the PCI side of the bridge reads one or more double words—data types representing 32 bits or 4 bytes—from memory on the PCIe side of the bridge. The amount of data the bridge buffers is typically more than what the PCI device initially requests. When using the blind-prefetch feature, some bridges burst as much as 4 kbytes of data in a single transaction, whereas conventional PCIe-to-PCI bridges can transfer only one double word at a time during normal operation. Each double-word transfer requires some setup time to process the transaction, thus adding to the total latency through the bridge. The bridge's burst transaction minimizes the setup time and, ultimately, the latency to only one transaction. With blind prefetching, the initial latency penalty occurs only once for every 4 kbytes of transferred data. Therefore, the blind-prefetch capability allows for maximum read performance by minimizing the latency time for devices reading large amounts of sequential data through the bridge.

For PCIe-to-PCI reads, the memory-read request determines the number of bytes to read, and prefetching does not occur. However, for PCI-to-PCIe reads, prefetching occurs in the prefetchable space for all memory-read commands, including memory read, memory-read line, and memory-read multiple, that the PCI bus issues. The prefetchable-memory-base and limit-configuration registers determine whether to forward

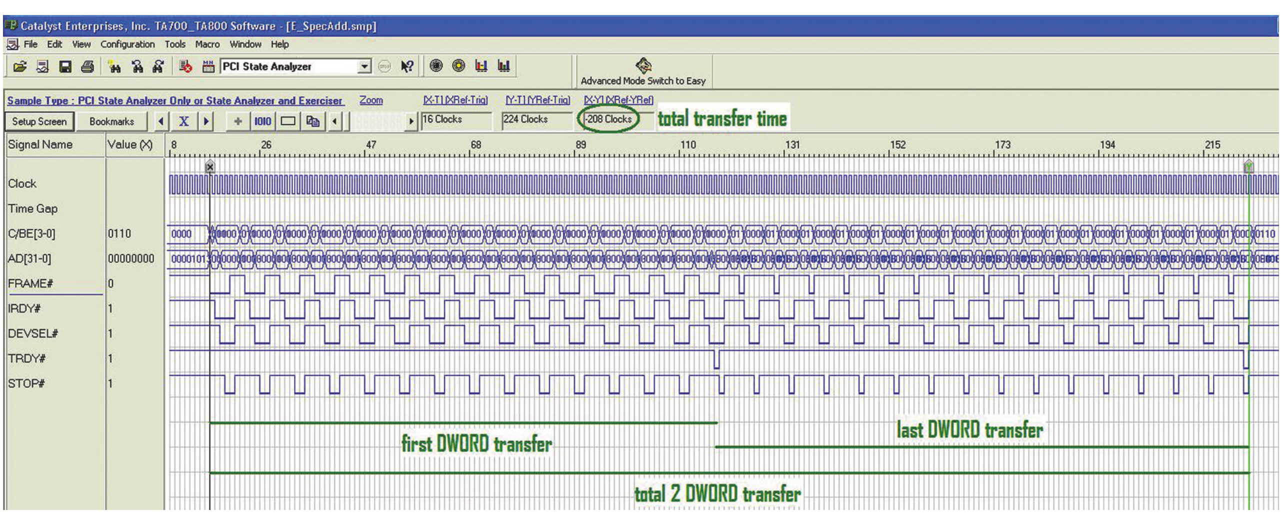

Figure 1 A two-double-word memory-read transaction without blind prefetch requires 208 clock cycles to complete.

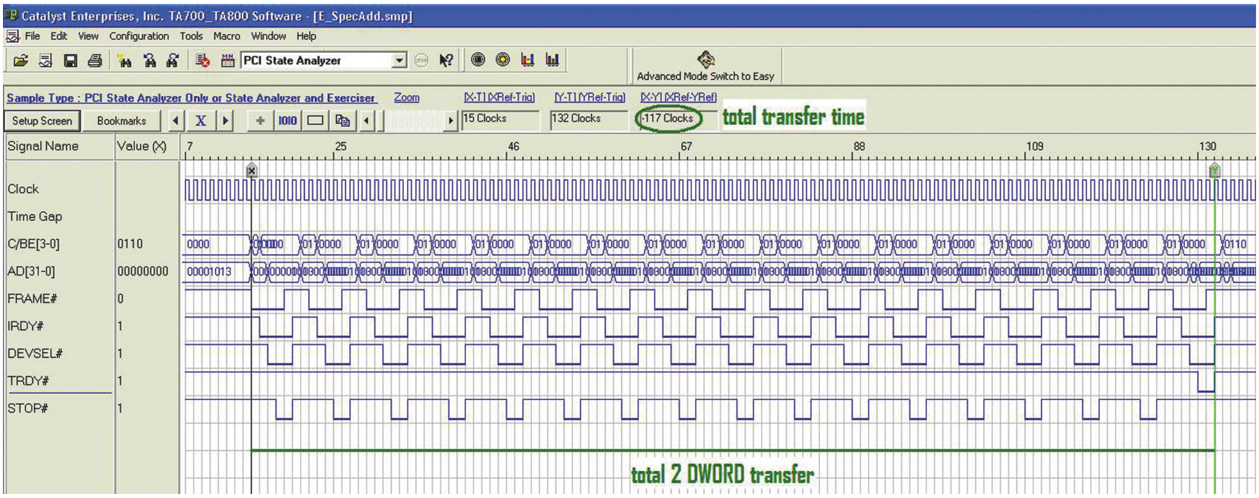

Figure 2 With blind prefetch, a two-double-word memory-read transaction finishes in 117 clock cycles.

prefetchable-memory transactions across the bridge. The primary bus forwards memory transactions that fall within the range that the prefetchable-memory-base and limit-configuration registers define. The secondary bus receives these transactions downstream, and the bridge ignores the memory transactions on the secondary bus that are within the range. The primary bus ignores memory transactions that do not fall within this range and forwards them upstream from the secondary bus provided they are not in the address range that the set of memory-mapped I/O-address registers defines or that the VGA (video-graphics-array) mechanism forwards downstream. For prefetching to occur, memory-read commands

must support the blind-prefetch feature. This feature greatly improves read performance because the bridge can burst its prefetchable data onto the PCI bus whenever the endpoint requests it.

Figure 1 shows a two-double-word transfer without blind prefetch. It takes 208 clock cycles for the transaction to complete from when you first assert the frame command. The transfer separates into two one-double-word transfers: The TRDY# (transfer-ready) signal asserts twice, and each assertion is only one clock cycle. Each transfer inherits a setup time, which ultimately adds to the increased latency through the bridge. **Figure 2** depicts the same two-double-word with blind prefetch. The total transfer time improves to only 117 clock cycles, from 208 cycles. Although the two-double-word transfer still breaks down into two separate transactions, the TRDY# signal asserts once for two clock cycles but with only one setup time for the whole transaction.

The two-double-word transfer saves 91 clock cycles, delivering a 44% increase when using the blind-prefetch capability of a PCI-to-PCIe bridge. Therefore, the blind-prefetch feature reduces latency by nearly 80% when transferring 4 kbytes of data in PCI-to-PCIe designs and enables a fivefold increase in transfer rate over normal operation.

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A number of the PCI-to-PCIe bridges now on the market implement the prefetching algorithm by simply configuring the blind-prefetch-enable bit in the device-specific-control register. This approach enables a memory-read command on the PCI bus, allowing the PCIe memory space to read at least one cache line from the PCIe interface. The bridge can read additional double words carrying 0 to 4 kbytes of data by setting the PCI-control-register programmed-prefetch-size field.

To maximize the bridge's read prefetch size, you must follow the following steps:

1. Set the maximum-read-request-size field in the PCIe device-control register to the maximum of 4096 bytes.
2. Set the programmed-prefetch-size field in the PCI-control register to the maximum of 4096 bytes.
3. Set the PCI-bus-latency-timer register to FFh to ensure that the host does not prematurely release the bus. In forward-mode designs, you may need to increase the PCI-latency timer of the bridge's downstream PCI-bus master, secondary PCI-latency timer, or both to ensure that the device does not prematurely release the bus. The precise values depend on the traffic pattern.

The maximum-read-request size defines the upper limit of the programmed-

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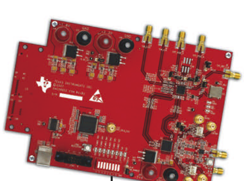

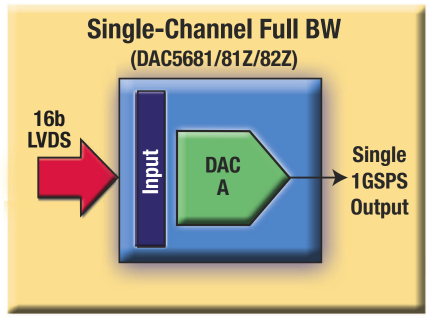

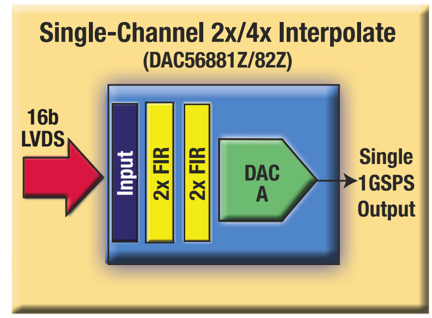

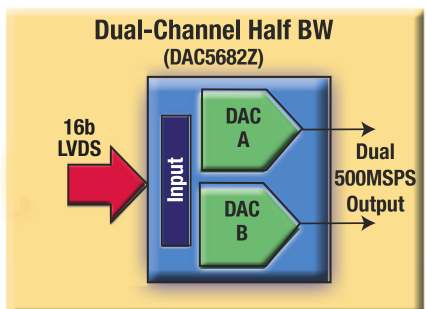

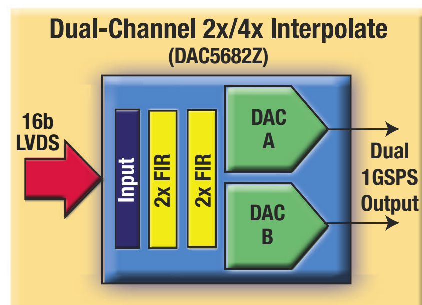

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Device	Number of DACs	Optional Digital Features				Power (typ)
		4xFIR	2xFIR	Mixer	PLL	
DAC5682Z	2	Yes	Yes	Yes	Yes	1400mW
DAC5681Z	1	Yes	Yes	No	Yes	800mW
DAC5681	1	No	No	No	No	650mW

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prefetch size, and the programmed-prefetch size is less than or equal to the maximum-read-request size. Program the maximum prefetch size to the largest possible for the transfer without exceeding the transfer size. If the prefetch size is greater than the number of bytes the bridge is reading, the reading and discarding of excess prefetch data will affect performance. If you require a higher speed bus, you can adjust the PCI-bus frequency, or you can set the PCLKO clock-frequency field in the device-initialization register to a maximum frequency of 100 MHz.

To maintain optimum performance, the anticipated read-burst size on the PCI bus must closely match one of the programmed-prefetch-size settings of the bridge. If the read-burst size is significantly smaller than the programmed-prefetch size, the bridge must discard the unused data after each read. This approach can negatively impact read performance by generating extra delay. Also, varying the read-burst size can affect the performance for some read transactions. In an ideal situation, the endpoint implements reads as bursts through DMA control, so that the read-burst size is fixed or controllable.

With multiple vendors offering a new generation of PCIe-bridging devices, designers can extend the lives of and add performance to boards and systems based on the conventional PCI bus. These PCI-to-PCIe migrations are introducing design complexities that advanced functions, such as blind prefetching, can alleviate. Designers with an understanding of such functions can minimize development efforts and time to market for the next generation of PCIe-based systems.**EDN**

AUTHOR'S BIOGRAPHY

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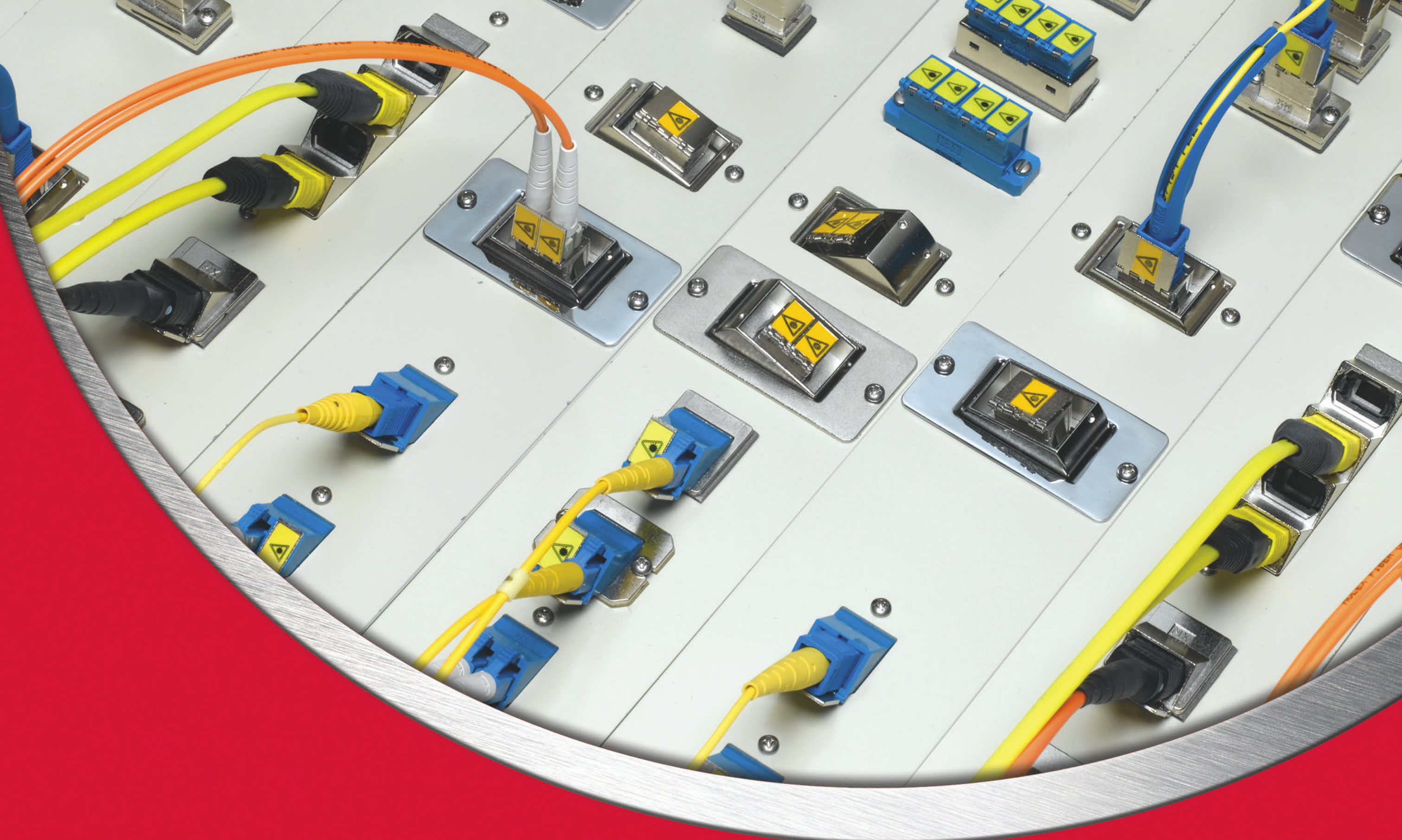

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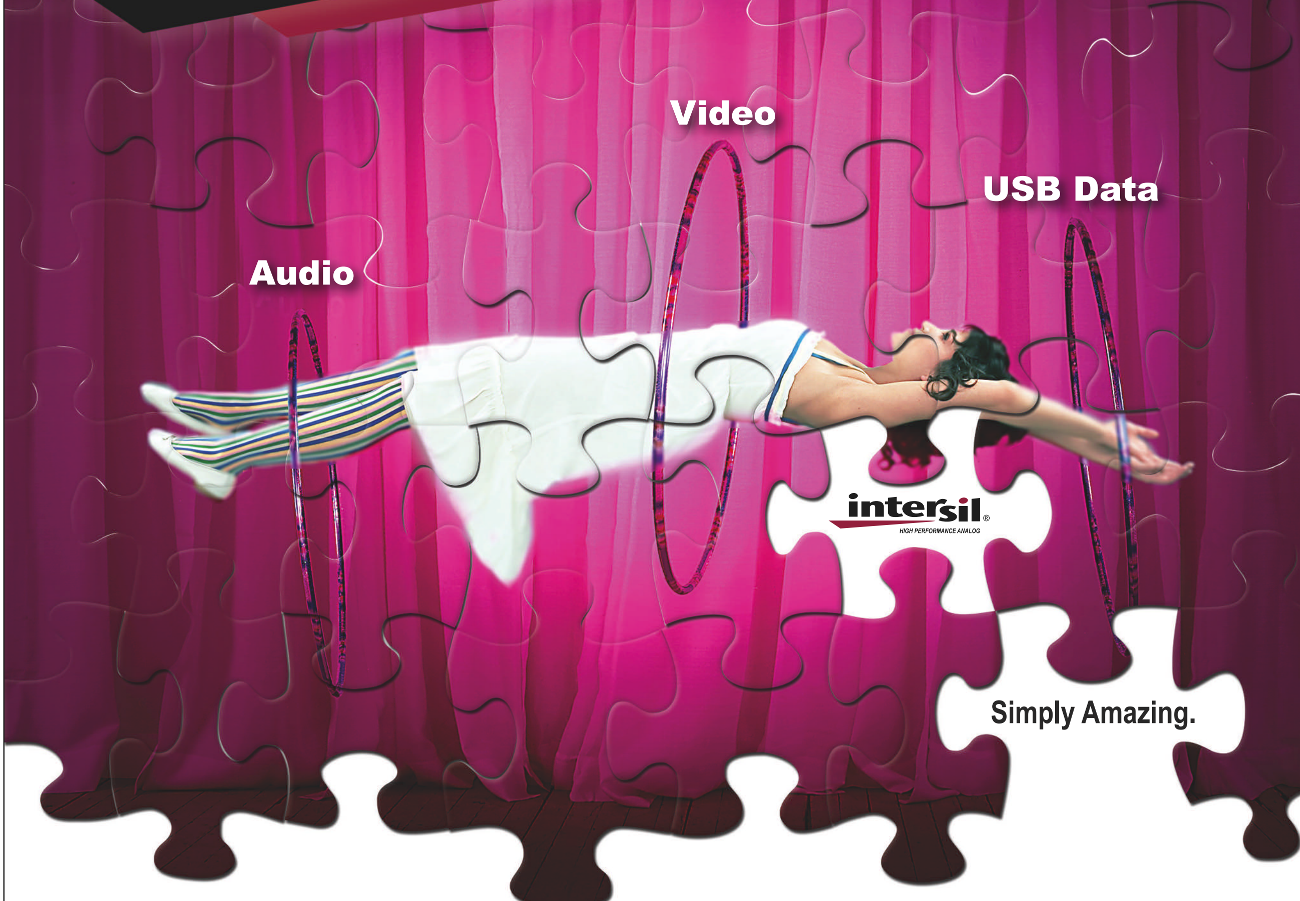

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Device	Audio THD 32Ω (%)	USB Speed	Video Diff Gain Phase
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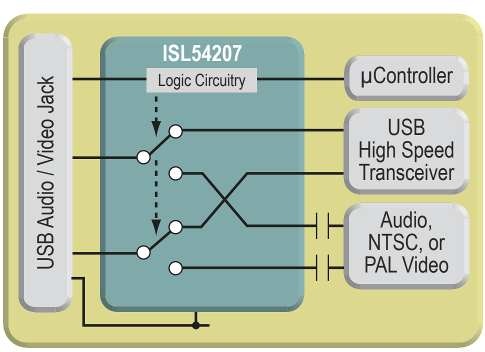
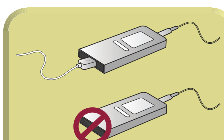
ISL54208	0.06	480	0.28 / 0.04
ISL54415	0.007	12	0.04 / 0.03
ISL54416	0.007	12	0.04 / 0.03
ISL54417	0.007	12	0.04 / 0.03





Combined data, audio, and video switch eliminates either the USB or TV OUT connector on cameras or media players.

Audio / Data

Device	Audio THD 32Ω (%)	USB Speed
ISL54205A	0.06	480
ISL54206	0.06	480
ISL54400	0.007	12
ISL54401	0.007	12
ISL54402	0.007	12

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A LETTER FROM THE EDITOR

In the late 1990s, technology was poised to "disintermediate" distributors from the rest of the supply chain. Internet technology would allow customers to order products directly from suppliers and enable suppliers to seamlessly fulfill these orders at no or little cost. If you are reading this article, you know this hasn't happened. Distribution still manages relationships among hundreds of suppliers and thousands of customers. True, consolidation means there are fewer distributors in the mix, but those that are on our 2008 list have survived the worst market downturn to date and have harnessed the Internet as a tool to actually improve customer relationships. One of the key functions distributors play in the supply chain is the delivery of new technologies from suppliers to customers. Distributors' salespeople and field applications engineers undergo extensive training sponsored by suppliers and by their own company. Per the Top 25 Electronics Distributors listing, No. 2 distributor Avnet, for example, builds reference designs that provide hands-on training for its engineers. No. 6 Newark and its parent Premier Farnell sponsors an annual design challenge called Live EDGE (Electronic Design for the Global Environment).

Energy efficiency represents one of the top opportunities for distributors going forward. European regulations are requiring energy-savings from products that use a wide range of electronics. Many products will require redesign in order to achieve these savings, so distributors have added to their sales force and realigned their applications engineers to assist designers. Distributors also target new channels for suppliers' products: light-emitting diodes (LEDs) are finding their way into the retail and building supply channels. The automotive market—traditionally limited to Tier 1 vendors and their suppliers—is also opening up for the channel. More electronics—and a wider array of devices—are going into automotive applications, so Tier 2 and Tier 3 vendors, heavy users of distribution, are making inroads in the automotive supply chain. These trends bode well for the channel, even in the current economic environment. Distributors aren't recession-proof, but spending on industrial electronics is less volatile than, say, consumer spending. And distributors have used technology to their advantage—tight profit margins have led to investments targeted at improving efficiency. As long as the channel remains a cost-effective means to reach thousands of customers, it will remain a vital link. ■

Freelance writer Barbara Jorgensen has been covering the electronics distribution industry for nearly 20 years, most recently as a Senior Editor at Electronic Business magazine.

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1	Arrow Electronics	8,586.0	15,900.0	17%	86.0%	P	A	54.0%	31.0%	15%(A)
2	Avnet	8,496.7	16,993.4	15%	2.2%	P	A	50.0%	31%(M)	19%(AJ)
3	Future Electronics[1]	3,662.8	5,232.5	15%	N/A	PR	A	70.0%	N/A	N/A
4	Bell Microproducts	1,701.0	4,050.0	19%	14.0%	P	A	42.0%	44.0%	0.0%
5	Digi-Key Corporation	771.7	941.1	14%	21.0%	PR	A	82.0%	8.0%	1.0%
6	Newark[3]	615.0	627.5	3%	N/A	P	A	98.0%	0.0%	0.0%
7	Nu Horizons	525.3	789.9	9%	18.5%	P	A	66.5%	8.5%	17.5%
8	TTI, Inc.	514.5	735.0	-29%	10.0%	P	A	70.0%	24.0%	6%(A)
9	DAC	480.5	485.4	2%	19.0%	PR	A	99.0%	0.0%	1.0%
10	Converge[1]	462.0	462.0	3%	N/A	PR	I	100.0%	0.0%	0.0%
11	Carlton-Bates[2,4]	374.0	374.0	10%	N/A	P	A	100.0%	0.0%	0.0%
12	Sager Electronics[1]	326.1	329.4	11%	N/A	PR	A	99.0%	1.0%	0.0%
13	Allied Electronics[2,5]	321.8	325.0	15%	N/A	P	A	99.0%	0.0%	0.0%
14	N. F. Smith & Associates	301.0	301.0	-26%	N/A	PR	I	100.0%	0.0%	0.0%
15	Richardson Electronics	227.4	554.6	-8%	N/A	P	A	41.0%	26.0%	30%(A)
16	Mouser Electronics	208.8	229.4	18%	33.3%	P	A	91.0%	4.5%	1.5%
17	America II Electronics	188.4	277.0	0%	N/A	PR	I	68.0%	16.0%	8.0%
18	Fusion[6]	170.0	200.0	6%	N/A	PR	I	85.0%	N/A	N/A
19	A.E. Petsche Co.	168.0	195.3	19%	20.0%	PR	A	86.0%	10.0%	1.0%
20	Dependable Component Supply[1]	157.0	257.3	5%	N/A	PR	I/A	61.0%	10.0%	23%(A)
21	JACO Electronics	132.0	203.0	-23%	4.0%	P	A	62.0%	10.0%	2.0%
22	PEI-Genesis	124.1	146.0	28%	23.0%	PR	A	85.0%	14.0%	0.0%
23	Advanced MP Technology[2]	105.7	302.1	14%	18.5%	PR	I	35.0%	25.0%	25.0%
24	Master Distributors	103.8	112.8	11%	N/A	PR	A	92.0%	2.0%	2.0%
25	Classic Components Corp.	99.6	249.0	1%	2.0%	PR	I	40.0%	27.0%	31.0%

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[1] Revenue figures and percentages are Reed Business Information estimates.

[2] Revenue figures are Reed Business Information estimates.

[3] Newark is parent company Premier Farnell's (West Yorkshire, England) main North American presence in electronic component distribution.

[4] Carlton-Bates is a subsidiary of WESCO Distribution.

[5] Allied is a subsidiary of Electrocomponents plc.

[6] North America revenue percentages are Reed Business Information estimates

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N/A	N/A	0.0%	12,600	1,261.9	70%	70%[A&P]	N/A	30%	0%	0%	0%	www.arrow.com
N/A	N/A	0.0%	12,350	1,376.0	N/A	36.0%	8.0%	56.0%	0%	N/A	0%	www.avnet.com
N/A	N/A	N/A	5,000	1,046.5	N/A	N/A	N/A	N/A	N/A	N/A	N/A	www.futureelectronics.com
0.0%	0.0%	14.0%	2,200	1,840.9	54%	20%	0%	75%	0%	5%	0%	www.bellmicro.com
1.0%	2.0%	6.0%	1,876	501.7	10%	39%	55%	0%	0%	0%	6%	www.digikey.com
0.0%	0.0%	2.0%	1,400	448.2	18.7%	13.7%	49.8%	9.7%	0%	0%	26.8%	www.newark.com
0.8%	0.0%	6.7%	809	976.4	75%	84%	8%	8%	0%	0%	0%	www.nuhorizons.com
0.0%	0.0%	0.0%	1,300	565.4	65%	0%	100%	0%	0%	0%	0%	www.ttiinc.com
0.0%	0.0%	0.0%	760	638.7	40%	0%	100%	0%	0%	0%	0%	www.heilind.com
0.0%	0.0%	0.0%	341	1,354.8	8%	80%	5%	15%	0%	0%	0%	www.converge.com
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0.0%	0.0%	1.0%	650	500.0	N/A	4.4%	54.2%	0%	0%	0%	41.4%	www.alliedelec.com
0.0%	0.0%	0.0%	318	946.5	0%	70%	24%	6%	0%	0%	0%	www.smithweb.com
N/A	N/A	3.0%	1,268	437.4	N/A	N/A	N/A	N/A	N/A	N/A	N/A	www.rell.com
1.0%	1.0%	1.0%	601	381.7	0%	33%	59%	0%	0%	0%	8%	www.mouser.com
2.0%	5.0%	1.0%	580	477.6	5%	72%	21%	2%	0%	5%	0%	www.americaii.com
N/A	N/A	N/A	70	2,857.1	N/A	80%	10%	10%	0%	0%	0%	www.fusiontrade.com
0.0%	1.0%	2.0%	313	624.0	9%	0%	100%	0%	0%	0%	0%	www.aepetsche.com
N/A	N/A	1.0%	N/A	N/A	18%	63%	35%	2%	0%	0%	0%	www.dependonus.com
2.0%	0.0%	24.0%	205	990.2	N/A	54%	21%	0%	0%	0%	25%	www.jacoelectronics.com
0.0%	0.0%	1.0%	438	333.3	70%	0%	100%	0%	0%	0%	0%	www.peigenesis.com
0.0%	5.0%	10.0%	215	1,405.1	10%	60%	30%	5%	0%	5%	0%	www.advancedmp.com
1.0%	1.0%	2.0%	169	667.5	14.0%	8%	73.0%	1.0%	18%	0%	0%	www.onlinecomponents.com
0.0%	0.0%	2.0%	300	830.0	3.0%	62%	34.0%	1.0%	0%	3%	0%	www.class-ic.com

**Distributors are ranked by calendar year 2007 North American revenue. N/A = Not available*
Revenue figures are gathered from financial filings, company provided information, and Reed Business Information estimates.

(A) IN ASIA PACIFIC
(M) INCLUDING MIDDLE EAST AND AFRICA
(AJ) IN ASIA INCLUDING JAPAN
(A&P) ACTIVE AND PASSIVE

Distributors Target Technology

What do the latest advances mean to the channel?

Without technology, the distribution channel as we know it today wouldn't exist. Electrical and radio technology paved the way for resellers in the early days; later, it was the microprocessor that drove the channel's growth. As technology continues to evolve at an ever-increasing pace, distributors embrace these advances to serve both suppliers and customers equally.

"Every aspect of our lives is significantly influenced by electronics," says Craig Conrad, senior vice president at TTI Inc., Fort Worth, TX (www.ttiinc.com). "The electronic content in everything from consumer products to white goods to military and aerospace continues to grow."

In particular, distributors and suppliers say, the evolving technologies most influencing their end markets today include energy-saving/green products; mobile technology/high-speed communications; medical/biotech equipment; and automotive electronics. These technologies are driving suppliers to develop new products and opening doors for distributors in both new and existing markets.

For example, Avnet Inc., Phoenix, AZ (www.avnet.com) is beginning to support retail businesses such as Home Depot and Staples. Light-emitting diodes (LEDs)—which have been around in the industrial channel for a long time—are targeting applications ranging from signs to high-end equipment. LEDs are not only energy efficient, but have a longer lifespan than traditional products. "Various market surveys have established LED market opportunities have been growing rapidly in the areas of architectural, signage and illumination lighting," according to Andy Wong, senior director, segment marketing and design services, Avnet EM Asia. "With recently rising energy costs and the immediate call for a greener environment globally, solar panels and low-power LED lighting ideal for emerging markets."

LEDs, however, aren't mainstream for the consumer market, so industrial distributors have an opportunity to step in and share their expertise. "Some of our accounts are completely new customers," says Marc Gsand, vice president, marketing, Avnet Electronics Marketing Americas. "We have a separate salesforce and experts called 'illumineers' to support the LED market," says Gsand.

GOING FOR THE GREEN

Energy efficiency is being mandated by the European Union so many electronics products may need to be redesigned in order to be compliant. The EU's Energy Using Products (EUP) mandate aims to improve the environmental performance of products through lower power consumption. This is raising the profile of new energy technologies such as switch-mode power conversion, integrated ICs, efficient transistors such as MOSFETs, resonant switching and synchronous power rectification.

Design engineers haven't typically been focused on issues such as energy-savings and recyclable products, says Gary Nevison, director of legislation and environmental affairs for catalog distributor Newark. (www.newark.com) Distributors can capitalize on this trend by providing up-to-date information on mandates, new products and by aiding design engineers in their product choices. "Engineers are looking for reliable sources of information," says DeWight Wallace, president of Newark. "It's also important to the design engineer that product be immediately available. They need a few devices and they need them right away. You have to be competitive by price, but also offer a solid value proposition."

Advances in the telecommunications industry are driving investment in both infrastructure and end-products. Speed and efficiency are key to supporting demand for both wired and wireless communications. "Today there are many developments that use high-speed interconnect from embedded systems to external interfaces," says Avnet's Wong. "These are RapidIO, XAUI, USB, HDMI, etc, just to name a few. High-speed serial interconnect is the technological milestone that marks the shift away from parallel data buses. High-speed serial interconnect is the answer to ease the signal congestion issues that designers are facing. This change is driven by the industry to meet system cost and systems scalability. With the advancement of silicon technology and shrinking of silicon geometry, it has enabled ease of adoption for high-speed serial interconnect at multi-gigabit rate to replace traditional parallel architecture."

Demand continues to increase for mobile technologies that deliver voice, video and text to both personal and automobile-based devices. Customers are looking for data delivery at speeds faster than conventional 3G mobile service and carriers are looking for services that are cheaper to implement using newer, more efficient technology. Customers want the ability to make phone calls, send an instant message, get travel information or access the Web—all by voice. With more advanced speech recognition, foldable screens and e-paper displays will replace traditional keyboards and monitors.

The U.S. will be one growth area for this technology, market watchers say. "After being eclipsed by Japan, South Korea and Europe in terms of advanced mobile handset features in recent years, U.S. consumers finally are embracing more sophisticated phones," said Greg Sheppard, chief development officer at market researcher iSuppli Corp. "This is having a major impact on the global competitive landscape of the wireless business."

THE AMAZING SHRINKING EQUIPMENT

As component footprints become smaller and smaller, end products are shrinking as well. Big items, such as medical equipment and instrumentation fall into this category. "High-end medical equipment and security equipment—traditionally expensive and big—is becoming portable and handheld," says Avnet's Gsand. In addition to consuming more and smaller components, this type of product hits another sweet spot for distributors and suppliers, says Eric Sussman, director of distribution, Americas, for Molex Inc., Lisle, IL (www.molex.com) "We are seeing a lot of opportunity in medical equipment—custom products for business that will stay in North America."

Displays are also getting integrated into this kind of equipment and finding other new applications. Screens are getting smaller and are improving in quality. "High-end graphics are available on small form factors so devices that previously had no displays can now use them," says Gsand. "The silicon driving the displays is also better; even in low-end LCDs the brightness of the light and the view of the display is incredible. Refresh times are getting better, so this has enabled displays to be integrated into lots of additional products."

The small/medium display market posted a great year in 2007, reports iSuppli. For the first time in many years, the pricing situation improved for displays with diagonal dimensions 10-inches or less in size due to healthy demand from applications that use such screens, including mobile handsets.

"Beyond just prices stabilizing in 2007, some prices actually increased and many companies enjoyed healthy quarterly results in the fourth quarter," said Vinita Jakhanwal, iSuppli's principal analyst for mobile displays.

TECHNOLOGY TAKES TO THE ROAD

Many of these innovations—smaller components, mobile technology, better displays—are all converging into automobiles. Although the auto industry remains a demanding customer, auto companies need electronics experts for a variety of reasons. By some accounts, the automotive market is becoming more accessible to electronics distributors. "It used to be in automotive: unless

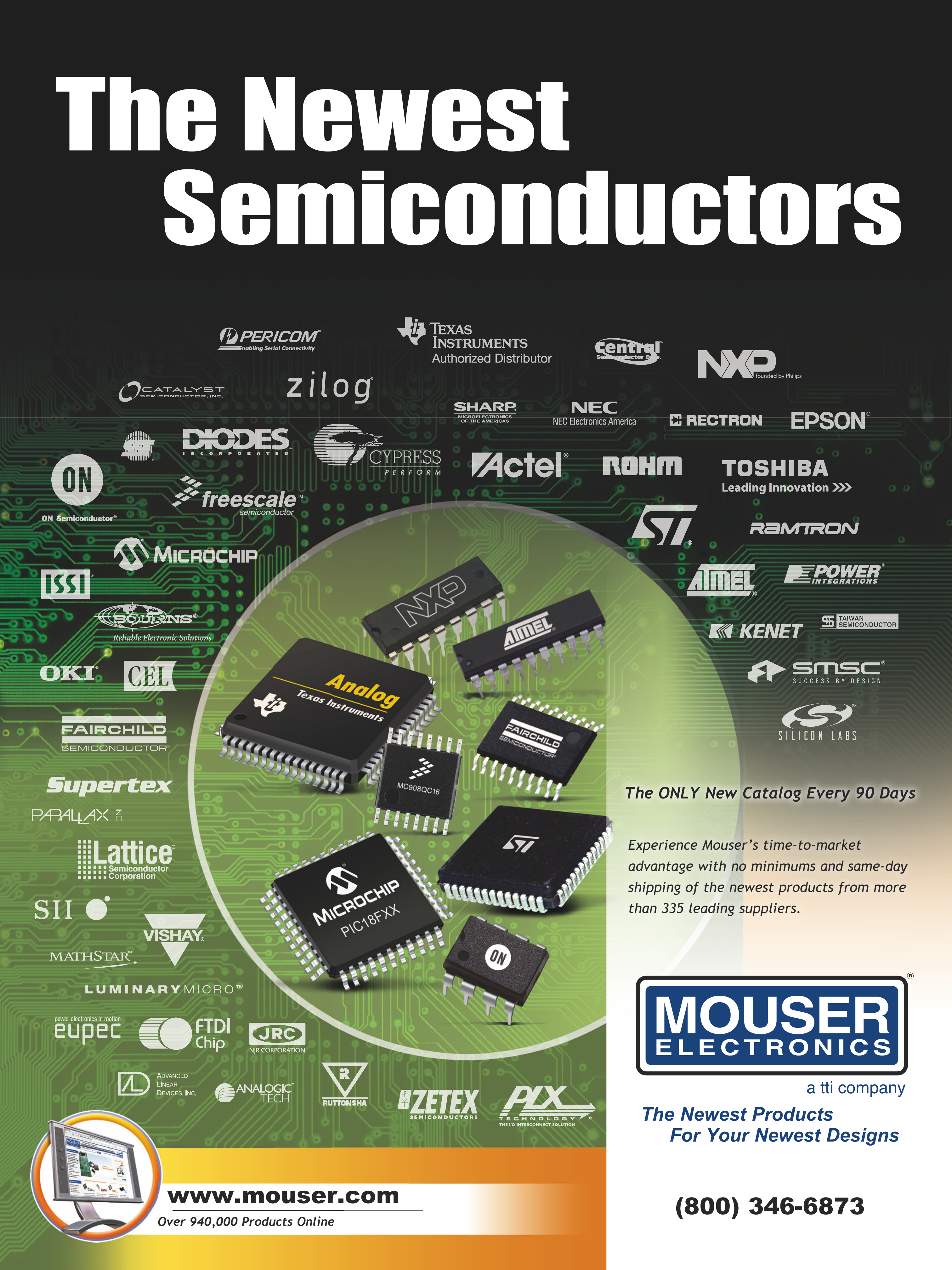
Application of Technology In The Channel

The National Association of Wholesaler-Distributors (NAW) polled distributors, manufacturers and customers on dynamics affecting the future. The NAW asked:

By 2006, will the biggest impact of technology be on the automation of wholesaler-distributors internal operations?

	PERCENTAGE OF RESPONDENTS		
	Unlikely	**Not sure**	**Likely**
Manufacturers	9%	12%	79%
Wholesaler/Distributors	6%	7%	87%
Customers	6%	14%	80%

SOURCE: NAW/Pembroke Consulting



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Texas Instruments
Authorized Distributor
Central Semiconductor Corp.
NXP founded by Philips
CATALYST SEMICONDUCTOR, INC.
zilog
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NEC
NEC Electronics America
RECTRON
EPSON
DIODES INCORPORATED
CYPRESS PERFORM
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you sold to the big Tier 1 suppliers you didn't play in that market," says Avnet's Gsand. "But with all the sensing and control functions that are being integrated [into autos], a lot of the car is being controlled and driven by Tier 2 and Tier 3 guys. What we are selling are complex and expensive solutions."

Suppliers already are looking at adjacent markets for growth. "We need to widen our sales opportunities to non-traditional markets beyond auto," says Molex's Sussman. Distribution, he adds, will play a leading role in Molex's growth plans.

"We have developed opportunity tracking documents with each of our five core distributors to monitor our success with customers in [Molex's targeted] areas. Distribution already has approached these account bases or has associated sales with non-competitive lines that we can develop a synergistic sell, "Sussman says.

TECHNOLOGY IN-HOUSE

One of the channel's biggest roles in the market is acting as a conduit of information between suppliers and customers. The channel has adopted the Internet as a major means of communication. "We have designed our Website so that engineers can find products easily, and with technical data sheets that supplement the supplier's data and provides technical support," says Newark's Wallace. "We've been ramping up so that we now have technical support offerings for second and third-tier customers as well." Newark also holds quarterly technology-focused seminars in product areas such as wireless and industrial.

Many distributors are realigning their sales forces and technical support by technology rather than by vendor. For example, instead of having an FAE that supports Texas Instruments or Analog Devices, FAEs are now DSP experts. This eliminates redundancies and makes better use of existing resources, says Avnet's Gsand.

Avnet is also reaching out to customers by building boards that focus on a particular function or solution. Avnet draws upon its wide vendor-based to mix and match components that provide the best solution, rather than designing a board around a specific vendor's product. Avnet also provides seminars on these designs, giving customers a "real-world" situation rather than referring to schematics.

The channel has also adopted technology to better serve customers and increase efficiencies. Distributors long ago began tackling the problem of tracking component designs and sales by developing proprietary software and computer systems. Since distributors derive most of their revenue from volume sales, it's imperative that they be able to capture that sale even if the design is done in the U.S. but product is manufactured in the Far East.

Wireless communications has also been adopted in the channel; distributors' salespeople use laptops, PDAs and other devices to keep abreast of customer developments in real-time. For example, if a distributor salesperson calls on a customer, he or she can access that customer's account; find what they have purchased in the past; where their account currently stands; and other relevant information. This kind of preparation not only saves both the distributor and customer time, but helps pinpoint up-and-coming products that the customer may want to use in future projects.

Technology is also aiding the channel in increasing efficiencies in-house. "Facing the Forces of Change," a study conducted by the National Association of Wholesaler Distributors, reports that the biggest impact technology will be on the automation of wholesaler-distributor internal operations (see chart).

THE BOTTOM LINE

So what are the implications for the channel going forward? Although the U.S. economy is expected to be challenging in the short-term, technology will continue to evolve. The electronics content in consumer items, white goods such as refrigerators, washers and dryers; automobiles; military and aerospace equipment; medical and test instruments and even in gasoline kiosks will continue to increase. Although dollar sales may not increase, distributors report unit sales and shipments are healthy.

Distributors' use of technology has made the channel healthier since the last industry downturn. In the middle of the first quarter of calendar 2008, inventory levels in the channel were in good shape, distributors and their suppliers report. This will help the channel avoid the type of inventory glut that happened in the 2001-2002 timeframe.

Nevertheless, 2008 will be a challenge. "The economy does have an impact on our business, especially as more of our business is driven off of consumer spending," says Jeff Newell, director, Americas Business operations for Dallas-based TI (www.ti.com). "Historically our industry has been more tied to IT spending and telecom infrastructure, but over the last few years we have seen a bigger piece of our business tied into consumer products. Should consumer spending wane, or more of our financial bellwethers go into a bad place, we could see a recession this year. My guess is that we will skirt the edges and come out of our economic funk in early 2009." ■


X-RAY
X-RAY

Up and Coming Technology Developments to Watch

Energy conservation efforts will drive distribution opportunities

The distribution channel has the unique distinction of bridging the gap between supplier products and end-market demand. As such, the electronics channel must exhibit in-depth knowledge of supplier products; demonstrate that knowledge to customers; and target end-market applications that represent the best opportunities for both suppliers and distributors.

Technology evolution not only drives the development of new markets for electronics; it strives to make products better, faster and more cost-effective. External trends also influence the direction technology takes. Currently, directives such as the European Union's Energy Using Products Directive (EuP), which mandates energy conservation measures in electronics products; pressure for better safety features in automobiles; and demand for engineering support and service present challenges and opportunities for the entire electronics supply chain.

ENERGY-SAVINGS/ ENVIRONMENT

Products targeting energy conservation and environmental-friendliness top the "up and coming technologies" list. The European Commission, says Gary Nevison, director of legislation & environmental affairs for catalog distributors Newark and Farnell, will be looking for energy savings from the following list of products:

- **Public street lighting; office lighting and domestic lighting**
- **Battery chargers and external power supplies**
- **Personal computers (desktops & laptops) and monitors**
- **Consumer electronics: televisions**
- **Domestic refrigerators and freezers**
- **Domestic dishwashers and washing machines**
- **Boilers and combi-boilers (gas/oil/electric)**
- **Water heaters (gas/oil/electric)**
- **Imaging equipment: copiers, faxes, printers, scanners, multifunctional devices**
- **Commercial refrigerators and freezers: chillers, display cabinets and vending machines**
- **Residential air conditioning and ventilation appliances**
- **Electric motors, water pumps (in commercial buildings, drinking water, food, agriculture) circulators in buildings and ventilation fans (non-residential).**

In order to achieve energy conservation, many products will have to be redesigned, Nevison says. This will not only require new breeds of components, but a higher level of support for design engineers. Engineers, says Nevison, are accustomed to designing products for performance, but not necessarily for recycling. Distributors are stepping up their efforts to not only supply product data but the kind of information that helps designers make informed product choices, says DeWight Wallace, president of Newark.

Some of the solutions the industry has to offer are familiar. Light-emitting diodes (LEDs) are smaller, longer-lasting and more energy efficient than fluorescent and other kinds of lights. LEDs have been used in industrial applications for many years but are now being used for signs and in buildings. In some cases, this means calling on non-traditional customers such as retail stores or construction suppliers and contractors. The industrial channel's familiarity with these products should be an advantage in these markets.

Batteries are another ubiquitous product playing a role in energy savings. "There is a lot of progress being made in battery life and power," says TTI Inc.'s Michael Knight, vice president, corporate product management and supplier marketing. "These improvements expand the need for many [existing] passive products, as well as drive the need for many new passive products. Examples include current sense resistors, power inductors, circuit protection and current and voltage regulation components, and high capacity/small form factor capacitors."

Also in this category are battery substitutes such as the new ultra capacitors that have similar cycling and discharge capabilities, Knight adds.


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Other new technologies that support energy savings, says Nevison, are switch-mode power conversion; integrated ICs; efficient transistors such as MOSFETs; resonant switching and synchronous power rectification.

TTI's Knight points out that market opportunities don't end with products designed specifically to save energy. The components that support these technologies on a circuit board are also in demand. "Regulations that mandate things like greatly reduced power draw when an electronic or electrical devices is hibernating or turned off, also increase the number of caps, resistors, filters, and inductors used in the power circuits within a stand-alone power supply, or on the power supply portion of a printed circuit card," he says. "In addition, these requirements are fueling the growth of an integrated solution from companies such as Power Integrations, On Semi, and ST Micro who are doing in silicon what a greater number of the discrete caps/resistors/inductors are being used for today."

TRANSPORTATION AND AUTOMOTIVE

Distributors say the automotive market is beginning to open up for Tier 2 and Tier 3 suppliers—the kinds of customers distributors have been calling on for a long time. "As vehicles of all kinds [cars to tractors] acquire an ever greater electronic content, and the companies who make them come under ever greater global economic and competitive pressures, manufacturing outsourcing is accelerating and fragmenting into different, specialized levels" says Knight. As the supply chains stretch and the number of contract manufacturers involved expand, the supply chain services of distribution all of a sudden become much more relevant and useful to this market segment, he explains.

"TTI is seeing an increasing level of interest from customers and electronic component suppliers in this space who would not have given us the time of day a few short years ago," says Knight. "We've built a team of subject matter experts who come from these industries and work across our local branch structures to provide tech support and training to our sales teams who have these customers in their territories. This group speaks the language, understands the applications, and knows how to match our suppliers offerings to these customers' needs."

Products that are finding wider use in the automotive market include sensors; microcontrollers; batteries; flash memory; MEMS; and networking devices.

MILITARY AND COMMERCIAL AEROSPACE

More and more components developed for the commercial marketplace are finding their way into military and aerospace applications. "Although we do not manufacture military products, commercial off-the-shelf parts are now widely used in military bills of material," says Eric Sussman, director of distribution, Americas, for Molex Inc. Distributors are looking to harness the technology advancements they've made in inventory management, supply chain and value-added services.

"These are important market segments to distribution," says TTI's Knight. "The electronic content continues to increase in complexity and deployment, even in things like tanks. Outsourcing, complex supply chains, and strong demand have made these segments very dependent on electronic component distribution."

TTI is responding by hiring program managers who know the market drivers and players and can help the distributor translate that information into inventory stocking plans and supply chain sales plans, he says. These managers also provide information to suppliers which help them to decide where to invest in capacity expansion. "Our military /aerospace business in North America could reach 30% of the total when all of the product we sell into the EMS sector, for mil/aero applications, is considered," says Knight. "On the connector side, the inventories and assembly services that distribution is maintaining in mil circulars is providing a critical buffer between the customers and a group of suppliers that basically run as job shops."

Finally, one of the more unusual developments distributors will be keeping an eye on is the role of software. Increasingly, says Marc Gsand, vice president of marketing, Avnet Electronics Marketing, Americas, "software is a big issue. Traditionally, most designs were done by hardware engineers and topped off by software. Today, maximizing the performance of a chip requires software." It's unlikely distributors will be called upon to write software code, but customers are consulting Avnet about software, he says. "Customers are buying the same chip, but those that can manipulate the chip the best are looking to talk with software implementers at Avnet." Increasingly, he says, customers are looking for solutions that mix and match the best of hardware—and software. ■

Technology and Compliance

Harnessing Technology in the Channel

Technology isn't just an end-product for electronics distributors—it's also a way to remain competitive in a global market. Distributors have harnessed the technology advancements to better manage inventory, business processes and, more recently, compliance with regulations that have been imposed by both U.S. and foreign governments. Find out how distribution customers ranked technology services in the future; how are public and private companies using technology…and more!

The Impact of Technology Advancement on the Channel coverage continues online.
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BY VISHWAS VAIDYA • TATA MOTORS LTD

How to maximize application payload with a minimal machine-code footprint

LEARN HOW TO ANALYZE A TRADITIONAL ALGORITHM TO DRASTICALLY REDUCE THE MEMORY FOOTPRINT AND GENERATE PROCESSOR-FRIENDLY MACHINE CODE FOR A TYPICAL AUTOMOTIVE APPLICATION.

Automotive designers of vehicle subsystems are always scouting for novel ways to extract maximum value from minimum resources. Embedded-system designers for automotive-electronics systems have no other choice than to stuff the maximum number of functions into a minimal code footprint. This article, apart from revealing some tricks of the automotive-embedded-system trade, mainly highlights some clever techniques for replacing a bulky and inefficient code segment with a slim and efficient one.

A typical automotive-control application consists of many real-time control loops based on mathematical models of physical quantities, real-time phenomena, and control strategies. Because shoestring budgets do not allow the use of costly DSPs, automotive designers must resort to a data-driven approach for implementing math functions. Values of the math functions reside in memory as parameters of the input variables. **Figure 1** shows a function of two variables—throttle and engine speed, for example—stored as a 2-D look-up table. This approach allows a simple, low-cost, 8-bit microcontroller to emulate a complex math function.

Table 1 shows a sample function as an 8×8-entry look-up table, or "map," in automotive parlance. Note that each of the eight points for both axes serves as an index of the look-up table. Most functions are usually more complex, requiring a matrix of approximately 16×16 entries. A typical control loop derives its setpoints from such a math function. Adaptive proportional-integral controllers within the control loop use similar look-up tables for the proportional and integral parameters, so these parameters adapt themselves to system dynamics in real time. **Figure 2** shows the complete control loop, including setpoint generation, for controlling a valve opening in real time. A typical automotive application involves many such control loops. More complex math functions require maps with three or more dimensions. These maps depend on series of multiple inputs, such as barometric pressure, coolant temperature, and air temperature.

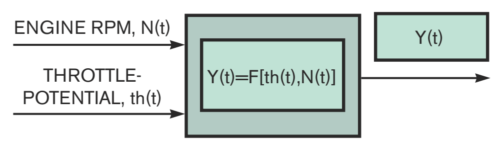

Figure 1 A 2-D look-up table stores a typical math function of two input variables.

The embedded code in such an application must access the map data by acquiring real-time inputs, such as throttle-usage percentage, engine speed, and coolant temperature, and then must use these inputs to perform a binary search that determines the row and column indexes of the maps. The code then accesses the maps to instantaneously obtain setpoints or proportional- and integral-control parameters. You repeatedly perform these steps in a control application; doing so optimizes this code and pays huge dividends in reducing the unproductive aspects of your application.

TABLE 1 SAMPLE FUNCTION

Throttle usage (%)	Engine speed (rpm)							
	700	900	1050	1600	2250	4300	5500	7550
0	13	23	100	0	0	51	52	0
10	18	100	34	0	0	0	0	0
25	0	0	0	0	32	11	0	0
40	76	0	0	63	0	100	100	100
55	0	54	0	0	0	100	100	100
70	5	0	12	18	32	84	100	100
85	0	0	0	0	42	100	100	100
100	0	0	0	0	0	0	0	100

The secret behind this reduction involves analyzing an assembly listing of the embedded C code and sometimes revisiting an algorithm to make it more digestible to a processor. Engineers with strong hardware backgrounds can easily identify the bulky assembly code. An in-depth postmortem analysis of the culprit code fragments in an assembly listing can uncover many useful concepts. For example, 8-bit compilers typically increase the code footprint when they must carry or borrow to account for results that might exceed 8 bits. Alternatively, you can make assembly code more efficient by using shifts and additions to replace routine arithmetic when feasible. Accessing a 2-D map using two indexes involves 8-bit multiplication with many carries, which gobbles up lots of code real estate. When possible, use a bit-set or -reset operation to replace arithmetic operations, such as bisection and averaging.

FINDING THE CULPRITS

You can use some tricks to detect and replace the culprit code. Consider a map of a 16×16-entry look-up table with

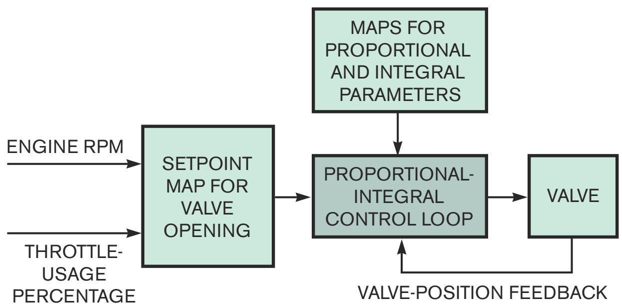

Figure 2 A typical automotive-control loop uses a proportional and integral controller.

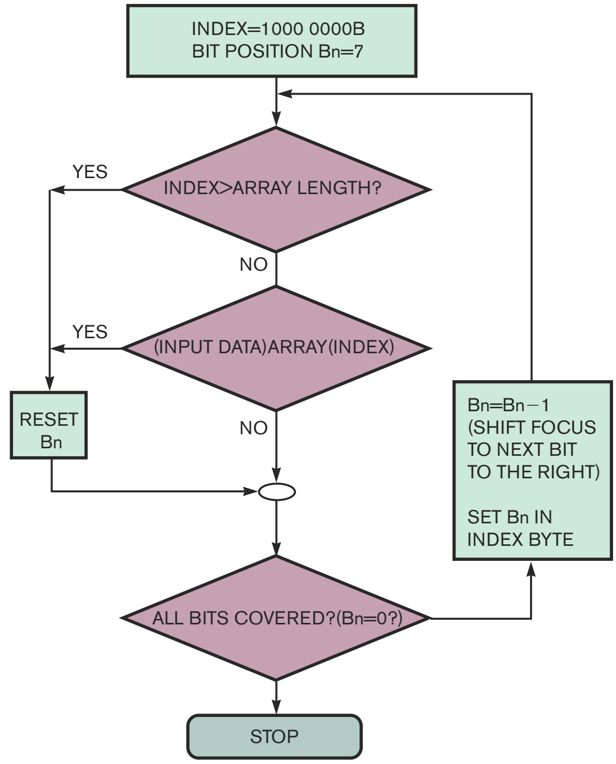

Figure 3 The bit-set/reset algorithm simplifies binary search of an array.

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a harmless-looking C statement: Data=Map (RowIndex, ColumnIndex);. This statement generates approximately 25 lines of assembly code. The 8-bit compiler treats the collection of the map's data points as a 256-element array. It computes the array index by performing lengthy 8-bit multiplication, considering a carry at every possible addition.

A smarter approach uses the fact that both row- and column-index would always be 4 bits; hence, a simple nibble concatenation would reduce the code down to six assembly lines. The trick lies in declaring a map as a single array of 256 elements in C code and using two C statements to access the map:

//Shift RowIndex by four and add ColumnIndex to obtain Data

MapIndex=(RowIndex<<4)+ColumnIndex;

Data=Map (MapIndex);.

The clever use of nibble shifting in RowIndex in effect performs multiplication by 16 to obtain MapIndex=16×RowIndex+ColumnIndex.

If you have an oddly dimensioned 10×11-entry map, you can-

TABLE 2 BIT-SET/RESET-BASED ALGORITHM FOR SMALLER CODE FOOTPRINT

No.	Traditional algorithm	Assembly lines	Bit-set/reset algorithm	Assembly lines	Remarks
1	Initializations	Three	Initializations	Three	
2	While statement	Five	While statement	Four	The traditional approach uses comparison.
3	Index=low+(low+high)/2	14	index |= array_mask	Two	In the heart of algorithm, the traditional algorithm proves most inefficient.
4	If (A(index)<value)low= index +1; else high=index-1	15	If (index>array_ length)index^=array_ mask	Six	You can omit six lines for the array-length comparison if the array length is an integer power of two.
			If (A(index)<value)index^=array_mask	10	
			array_mask >>= 1	Two	
5	Total lines	37		27	28% saving with new algorithm

not use a simple nibble-shift, but you can use multiplication by 10 without needing to perform tedious 8-bit arithmetic:

```
RowIndexInto2=RowIndex<<1;
RowIndexInto8=RowIndexInto2<<2;
RowIndexInto10=RowIndexInto8+
RowIndexInto2;
MapIndex=RowIndexInto10+
ColumnIndex;
MapIndex=(Row× (8+2)+Column)
Data=Map (MapIndex);
```

You achieve this multiplication using a simple shift-and-add operation, causing substantial savings in machine-code footprint.

Every map access requires two indexes that you obtain by performing an index search. Consider the map in **Table 1**. If the real-time-input values for the engine's speed and the throttle-usage percentage are 1250 rpm and 45%, respectively, the row index should be five, and the column index should be four. Most popular binary-search algorithms use progressive bisection to zero in on the final index. **Listing 1** at www.edn.com/080417ms4278 gives the traditional approach. When applying **Listing 1**, assume a 250-array element with a low of zero and a high of 250. The algorithm continues to bisect the search interval and evaluates both halves to see which one of them contains a match. The "winning" half becomes the new and smaller search interval for the next iteration until you find the closest match. You can use this traditional algorithm for reducing your code footprint. Obvious culprits are lines such as index=low+(low+high)/2, which contains two additions and one division. The while statement, while (low≤high), embeds some less obvious hidden devils.

This process again involves using the compiler to perform 8-bit arithmetic. **Listing 2**, available at www.edn.com/080417ms4278, produces a smaller version of the code footprint. It uses the same "divide-and-conquer" theme, except that, this time, the division is processor-friendly. You initialize the search index to zero. Then, assuming an array length of 128 to 255, you set the most significant bit of the index to one to access the 128th element of the array and compare it with the input data. Depending on the outcome of the comparison, you either reset the bit or leave it at one. This approach selects the winning half as the next search interval. You also reset the bit if the index formed after setting the bit is out of range. This scenario does not occur if the array length is an integer power of two. The next iteration sets the next bit to the right, yielding an index of 1100 0000b or 0100 0000b, depending on the outcome of the previous iteration. Each iteration progressively determines the value of the next bit toward the least significant bit. Electronics engineers familiar with the hardware concepts of analog-to-digital conversion will appreciate that this algorithm in effect adopts the successive-approximation philosophy of an ADC.

Figure 3 shows the flow chart for this progression, and **Table 2** shows the equivalent assembly-code lines that


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Hi-Tech Software's (www.htsoft.com) C compiler for a Microchip (www.microchip.com) PIC16F77 microcontroller produces. All the operation involving direct and indirect arithmetic operations can liberally consume the code space. Thus, a while statement with comparison occupies five lines compared with a bit-based approach that occupies only four. The main culprit for the larger footprint is: index=low+(low+high)/2, which generates 14 lines compared for two lines with bit set/reset.

This example amply proves how a face lift on a worn-out algorithm can gain you quite a few bytes of code space. As **Table 2** shows, the new algorithm saves 28% in code space. If the array length is an integer power of two, you can omit the out-of-range check of the index, saving six more assembly lines for a total savings of 43%.

This article highlights basic approach to remove unproductive "fat" from your embedded application. The key lies in the analysis of the assembly listings, as the binary-search example amply illustrates. Apart from saving machine space, a significant by-product of this strategy happens to be the faster execution resulting from a small-footprint-code execution. You may discover new tricks by reviewing the assembly listing of your C code and attacking the bulky code fragments.EDN

AUTHOR'S BIOGRAPHY

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DESIGN NOTES

Signal Chain Noise Analysis for RF-to-Digital Receivers

Design Note 439

Cheng-Wei Pei

Introduction

Designers of signal receiver systems often need to perform cascaded chain analysis of system performance from the antenna all the way to the ADC. Noise is a critical parameter in the chain analysis because it limits the overall sensitivity of the receiver. An application's noise requirement has a significant influence on the system topology, since the choice of topology strives to optimize the overall signal-to-noise ratio, dynamic range and several other parameters. One problem in noise calculations is translating between the various units used by the components in the chain: namely the RF, IF/baseband, and digital (ADC) sections of the circuit.

Figure 1 shows a simplified system diagram. There is an RF section, an IF/baseband section (represented by an amplifier) and an ADC. The RF section, which includes a mixer or demodulator, is commonly specified using noise figure (NF) in a decibel scale (dB). This may also be specified with a noise power spectral density which is similar to NF in concept (e.g., –160dBm/Hz is equal to an NF of approximately 14dB), so here we use NF. When working in a fixed-impedance (50Ω) environment, using NF simplifies the analysis of an RF signal chain. However, if the assumptions of constant impedance and proper source/load termination are not valid, then NF calculations become less straightforward.

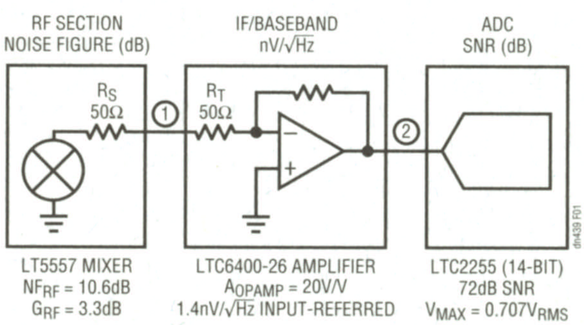

Figure 1. Block Diagram of a Simplified Signal Chain with RF Components (Mixer, LNA, etc.), IF/Baseband Components (Represented by a Simple Amplifier) and an ADC. The Input Resistor of the Amplifier Serves as a Matched Termination for the 50Ω RF Section. A Suggested Product, and Its Specification for Each Section, Are Included

IF/baseband components, such as amplifiers, are typically specified with noise spectral density, which is commonly measured in volts and amps per square-root Hertz ($nV/\sqrt{Hz}$ and $pA/\sqrt{Hz}$). The contribution of current noise ($pA/\sqrt{Hz}$) is usually negligible in low impedance environments. ADC noise is primarily specified as a signal-to-noise ratio (SNR) in decibels. SNR is the ratio of the maximum input signal to the total integrated input noise of the ADC. In order to perform a full signal chain analysis, a designer needs to be able to translate between NF, noise density and SNR.

NF to SNR: How Much ADC Resolution?

The first transition is from the RF section to the IF/baseband section. NF is a convenient unit, but requires constant system impedance. Since noise spectral density is independent of impedance, converting from NF to $nV/\sqrt{Hz}$ makes sense, since in the transition from RF to baseband (node 1 in Figure 1), the chain is leaving the fixed 50Ω environment. At node 1, the noise voltage density due to the RF part of the chain can be represented as:

$$e_{N(RF)} = 10^{\left[\frac{(G_{RF}+NF_{RF})}{20}\right]} \bullet e_{N(50)} \bullet 0.5\left(\frac{nV}{\sqrt{Hz}}\right)$$

where G_{RF} = cascaded gain of RF component(s) in dB

NF_{RF} = cascaded NF of RF component(s) in dB

$e_{N(50)}$ = noise density of 50Ω ($0.91nV_{RMS}/\sqrt{Hz}$ at 27°C)

0.5 = resistive divider from load termination, equal to 0.5 if R_T and R_S are 50Ω.

With the LT5557 shown in Figure 1, $e_{N(RF)}$ comes out to 2.25nV/$\sqrt{Hz}$. The input-referred voltage noise density of the IF/baseband section (including op amp resistors) can be computed using the op amp data sheet and summed with the contribution from the RF portion (using sum-of-squares addition since the specified values are RMS). Multiplying the result by the amplifier gain (V/V) gives the total noise density at node 2, ignoring the ADC's effective contribution:

$$e_{N2} = A_{OPAMP} \bullet \sqrt{e_{N(OPAMP)}^2 + e_{N(RF)}^2} \left(\frac{nV}{\sqrt{Hz}}\right)$$

Using the LTC6400-26 amplifier's specifications, e_{N2} comes out to 53nV/$\sqrt{Hz}$. The final step is to compute the overall SNR at the ADC. To do so, one must know the total integrated noise at node 2. Assuming the noise spectral density is constant with frequency, one can simply multiply e_{N2} by the square root of the total noise bandwidth. This bandwidth is limited by the amplifier circuit and any ADC antialias filtering. Assuming a total bandwidth of 50MHz, the integrated noise in our example is N2 = 375µV_{RMS}. The total theoretical SNR can be calculated as:

$$SNR_{THEORETICAL} = 20 \bullet \log_{10}\left(\frac{V_{MAX}}{N2}\right)(dB)$$

where V_{MAX} = maximum sine wave input to the ADC in V_{RMS} ($V_{P-P} \bullet 0.35$)

N2 = total integrated noise at node 2, excluding the ADC, in V_{RMS}

This theoretical SNR, which is 65.5dB in the example, represents the maximum resolution attainable with a perfect ADC. The actual ADC should have an SNR at least 5dB above this number to maintain the performance level down the chain. For example, a practical high performance 14-bit ADC, like Linear Technology's LTC2255 family (or LTC2285 family of dual ADCs), would have an SNR in the 72dB to 74dB range.

SNR to NF

For radio designers, an important consideration in system design is total noise figure, which is affected by all components in the chain. Once the components are selected, one can determine the equivalent input noise figure and the overall sensitivity of the receiver. Assuming that the signal(s) of interest lie within one Nyquist bandwidth of the ADC (a Nyquist bandwidth is $f_{SAMPLE}/2$), the equivalent noise of the ADC is:

$$e_{N(ADC)} = 10^9 \bullet \frac{V_{MAX}}{10^{\left(\frac{SNR_{ADC}}{20}\right)}} \bullet \frac{1}{\sqrt{\frac{f_{SAMPLE}}{2}}} \left(\frac{nV}{\sqrt{Hz}}\right)$$

where SNR_{ADC} = data sheet SNR at the frequency of interest in dB

f_{SAMPLE} = sample rate of the ADC in Hertz

In our example, $e_{N(ADC)}$ comes out to 22.5nV/$\sqrt{Hz}$, assuming a 125MHz sample rate. This voltage noise density, $e_{N(ADC)}$, can then be RMS-summed with the amplifier output noise density, e_{N2}, and the result input-referred by dividing by the gain, A_{OPAMP}. To convert back to NF, rearrange the first equation in this article:

$$NF_{TOTAL} = \left\{20\log_{10}\left(\frac{\sqrt{e_{N(ADC)}^2 + e_{N2}^2}}{A_{OPAMP} \bullet e_{N(50)} \bullet 0.5}\right) - G_{RF}\right\}(dB)$$

This quantity, NF_{TOTAL}, gives the overall input noise figure with the contributions of the RF section, the amplifier and the ADC. In the example, NF_{TOTAL} is 12.7dB for the entire chain of three devices.

Conclusion

When working with an entire system design from RF components to ADC, noise specifications do not always use the same units from component to component. This article addresses the translation between the various nomenclatures. Radio designers can use this information to design their system topology and select components for optimal sensitivity.

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LTC3562	600mA + 600mA + 400mA + 400mA				3 x 3 QFN-20
LTC3445	600mA			50mA + 50mA	4 x 4 QFN-24
LTC3670/72	400mA			150mA + 150mA	2 x 3 DFN-12 / 2 x 2 DFN-8
LTC3100	250mA	800mA		100mA	3 x 3 QFN-16
LTC3446	1A			300mA + 300mA	3 x 4 DFN-14
LTC3541	500mA			300mA	3 x 3 DFN-10
LTC3545	800mA + 800mA + 800mA				3 x 3 QFN-16
LTC3522	200mA		400mA		3 x 3 QFN-10
LTC3520	600mA		1A	LDO Controller	4 x 4 QFN-24
LTC3537		600mA		100mA	3 x 3 QFN-16
LTC3523	400mA	600mA			3 x 3 QFN-16
LTC3527		600mA + 400mA			3 x 3 QFN-16
LTC3547	300mA + 300mA				2 x 3 DFN-8
LTC3419	600mA + 600mA				3 x 3 DFN-10, MS10
LTC3548	800mA + 400mA				3 x 3 DFN-10, MS10E
LTC3407A-2	800mA + 800mA				3 x 3 DFN-10, MS10E
LTC3417A-2	1.5A + 1A				3 x 5 DFN-16, TSSOP-20E

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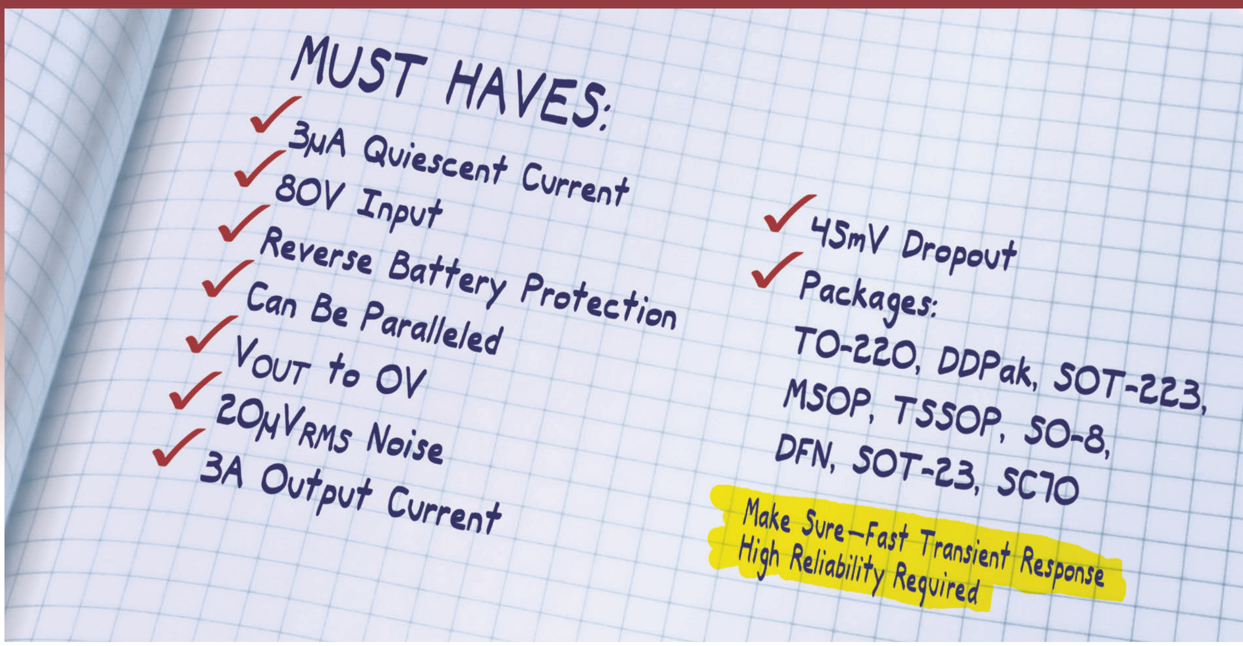
High Performance LDOs



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LT3010/H*	50mA/50mA	80	0.30	100	30µA	Adj. (1.275 to 60), 5	ThinSOT™
LT1761	100mA	20	0.30	20	20µA	Adj. (1.22 to 20), Fixed	ThinSOT
LT1762	150mA	6.5	0.30	20	25µA	Adj. (1.22 to 20), Fixed	MSOP-8
LT3012/H*	250mA/200mA	80	0.40	100	40µA	Adj. (1.24 to 60)	3 x 4 DFN-12, TSSOP-16E
LT3013/H*	250mA/200mA	80	0.40	100	65µA	Adj. (1.24 to 60)	3 x 4 DFN-12, TSSOP-16E
LT1962	300mA	20	0.27	20	30µA	Adj. (1.22 to 20), Fixed	MSOP-8
LTC®3025	300mA	5.5	0.05	80	54µA	Adj. (0.4 to 3.6)	2 x 2 DFN-6
LTC3035	300mA	5.5	0.045	150	100µA	Adj. (0.4 to 3.6), Fixed	2 x 2 DFN-6
LT1763	500mA	20	0.30	20	30µA	Adj. (1.22 to 20), Fixed	SOIC-8
LTC3025-1/-2	500mA	5.5	0.075	80	54µA	Adj. (0.4 to 3.6)/1.2	2 x 2 DFN-6
LT3080**	1.1A***	36 (40 Abs Max)	0.3+	40	1mA	Adj. (0 to 36)++	3 x 3 DFN-8, MSOP-8E, TO-220, SOT-223
LT1965	1.1A	20	0.29	40	500µA	Adj. (1.20 to 19.5)	3 x 3 DFN-8, MSOP-8E, TO-220, DDPak
LT1963/A	1.5A	20	0.34	40	1mA	Adj. (1.21 to 20), Fixed	DDPak, TO-220, SOT-223, SO-8
LT1764/A	3A	20	0.34	40	1mA	Adj. (1.21 to 20), Fixed	DDPak, TO-220

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READERS SOLVE DESIGN PROBLEMS

Use thermoelectric coolers with real-world heat sinks

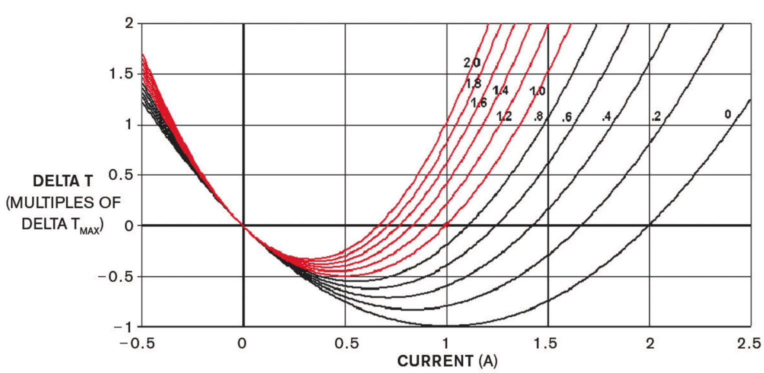
W Stephen Woodward, Chapel Hill, NC

Peltier devices, also known as solid-state refrigerators, or TECs (thermoelectric coolers), actively cool temperature-sensitive electronic components, such as optical detectors and solid-state lasers. A glance at any TEC data sheet reveals that some primary and fairly easily understood parameters characterize a TEC: The maximum current is the TEC's current drive for maximum cooling, the maximum differential temperature is the no-load cooling temperature at maximum current and with no heat load. The maximum voltage is the TEC's voltage drop at the maximum-current drive, and the maximum heat transfer (Q_{MAX}) is the maximum cooling-heat load at a maximum current and differential temperature of zero.

However, one TEC data sheet proviso that designers sometimes miss is that you always measure these parameters with the TEC mounted on an effectively zero-thermal-impedance—that is, perfect—heat sink. This point is an important one and deserving of the designer's rapt attention because heat sinks always have at least some thermal impedance, and all the primary TEC parameters change—sometimes dramatically—when the TEC must make do with an imperfect sink.

The family of impedance-versus-current curves in **Figure 1** illustrates this effect. Each curve corresponds to a different heat-sink thermal impedance, normalized to one for 11 values from zero to two.

Although the maximum current is, by definition, the optimal current for



NOTE: HEAT-SINK IMPEDANCE IS NORMALIZED TO: 1.0=DELTA T_{MAX}/Q_{MAX}.

Figure 1 This family of curves shows that a thermoelectric cooler may actually heat rather than cool at the maximum drive current if the heat sink the cooler is mounted on is less than perfect.

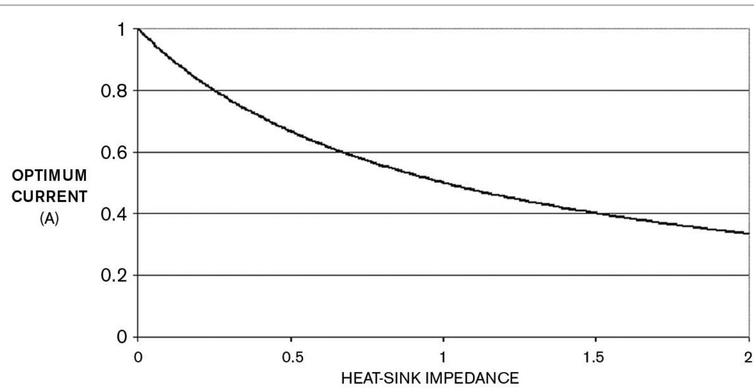


Figure 2 A derating factor for maximum voltage and current is based on the real-world thermal impedance of the TEC's heat sink.

DIs Inside

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maximum cooling at a heat-sink impedance of zero, the situation changes radically with increasing impedance until there's no net cooling whatsoever. Further, for impedance greater than one, instead of cooling, the maximum TEC drive actually heats rather than cools. **Figure 2** shows the simple solution for this problem: You must replace the data sheet's maximum current and voltage values with new, lower maximum-drive values corresponding to the optimal numbers you need to achieve maximum cooling whenever impedance is greater than zero. **EDN**

Interface MIDI instruments to a PC through a USB port

Stefano Palazzolo, Senago, Milan, Italy

This Design Idea uses the FT-232BM from Future Technology Devices International (www.ftdichip.com), a USB-to-UART interface IC that you need not program, to interface a USB port to the MIDI (musical-instrument-digital-interface) bus (**Figure 1**). The USB signals directly interface to IC_1, an FT232BM. The serial-transmitter and -receiver signals pass through IC_2 and IC_3 to transform the RS-232 signals to the MIDI's loop current. You can use an EEPROM, IC_4, if you want to add a serial-number interface or use more than one interface.

This hardware doesn't require you to write any software. However, you must install two drivers. First, you need the free VCP driver from FTDI at www.ftdichip.com/Drivers/VCP.htm. It allows you to use this interface as a common serial-port interface. Before you install it, you must change a string in the file FTDIPORT.INF (**Reference 1**) to set up the 31,250-baud rate for FT232BM. Then, you can configure VCP to run at 38,400 baud. (The real baud rate will be 31,250 as preset in FTDIPORT.INI.)

Then, you must install another driver that permits you to see your VCP serial port as a MIDI port for addressing all MIDI messages. You can find a lot of similar drivers on the Internet. For example, the Roland serial MIDI driver is available at: http://www.roland.it/dow_drivers/for_win/serial32_wxp2k.exe. You can enable this driver on the COM1 or the COM3 port.

Listing 1, at www.edn.com/080417di1, shows the changes to add to the FTDIPORT.INF file that change the baud rate from 38,400 to 31,250 baud. Change this file before installation. **EDN**

REFERENCE

1 "FT232BM Designers Guide, Version 2," FTDI, 2002/2003, www.ftdichip.com/Documents/AppNotes/DF232_20.pdf.

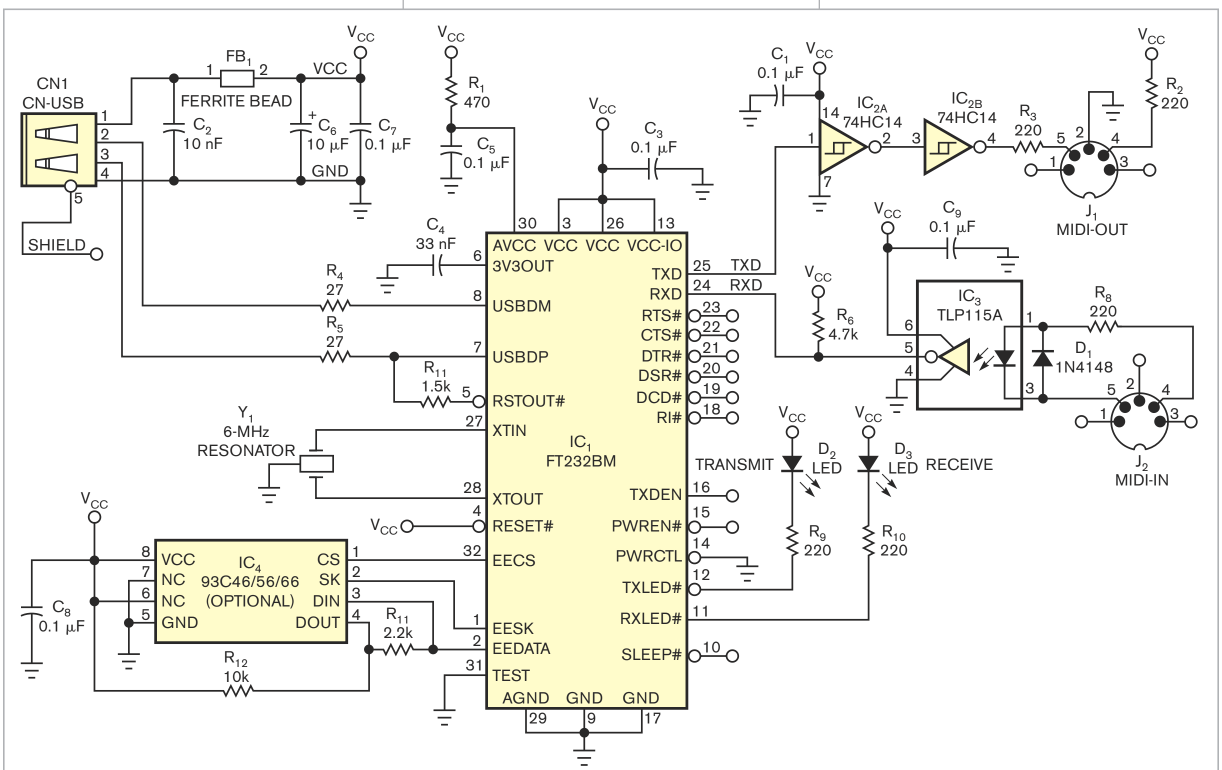
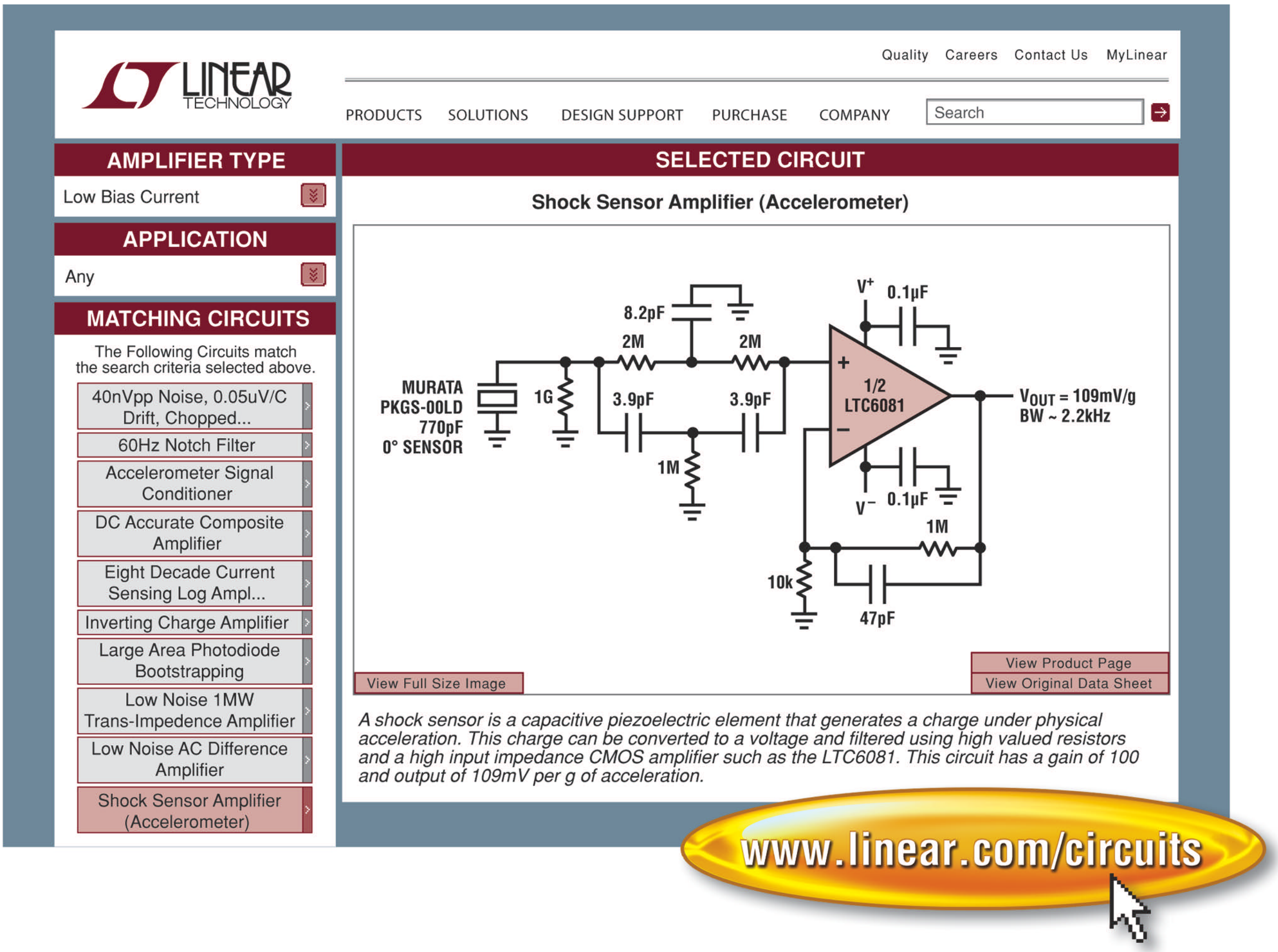


Figure 1 This USB-to-MIDI interface uses the FT232BM, a USB-to-UART interface chip that you need not program.

Op Amp Circuit Collection



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LTC6082	0.2	70	3.6	0.4	4	TCV_{OS} = 0.8µV/°C Max.	DFN-16, SSOP-16
LTC6087	1	750	14	1.2	2	General Purpose	MS-8, DFN-10
LTC6088	1	750	14	1.2	4	General Purpose	DFN-16, SSOP-16
LTC6078	0.2	25	0.75	0.072	2	TCV_{OS} = 0.7µV/°C Max.	MS-8, DFN-10
LTC6079	0.2	25	0.75	0.072	4	TCV_{OS} = 1.4µV/°C Max.	DFN-16, SSOP-16
LTC6240	0.2	175	18	2.4	1	Low Frequency Noise = 550nV$_{P-P}$	SOT-23-5, SO-8
LTC6241	0.2	125	18	2.2	2	Low Frequency Noise = 550nV$_{P-P}$	DFN-8, SO-8
LTC6242	0.2	150	18	2.2	4	Low Frequency Noise = 550nV$_{P-P}$	DFN-16, SSOP-16
LTC6244	1	100	50	5.8	2	Low Frequency Noise = 1.5µV$_{P-P}$	DFN-8, MS-8

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LINEAR TECHNOLOGY

Transmission lines simulate digital filters in PSpice

David Báez-López, Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada

Designers use PSpice mainly to simulate analog circuits. However, you can also simulate digital filters with it. The main components in a digital filter are delay elements, adders, and multipliers. Although you can implement adders and multipliers using operational amplifiers, you can simulate a delay element with a transmission line. The transmission line in PSpice is a long-forgotten element that can realize a delay of seconds.

For example, **Figure 1** shows a second-order recursive digital filter. The transfer function for this filter is:

$$H(z)=\frac{B_0z^2+B_1z+B_2}{z^2+A_1z+A_2},$$

where H(z) is the digital-filter-transfer function, *z* is the *z*-transform variable, the As are the coeffieients of the denominator polynomial of the transfer function, and the Bs are the coefficients of the numerator polynomial of the transfer function. You can obtain the coefficient values with software available for filter design (**Reference 1**). The sampling frequency, f_S, relates to the transmission-line delay as $t=1/f_S$. For example, a bandpass digital filter with a 3-dB passband from 900 Hz to 1 kHz, a sampling frequency of 6 kHz, and a Butterworth characteristic yields the following transfer function:

$$H(z)=\frac{z^2-1}{z^2-0.9096707z+0.809374}.$$

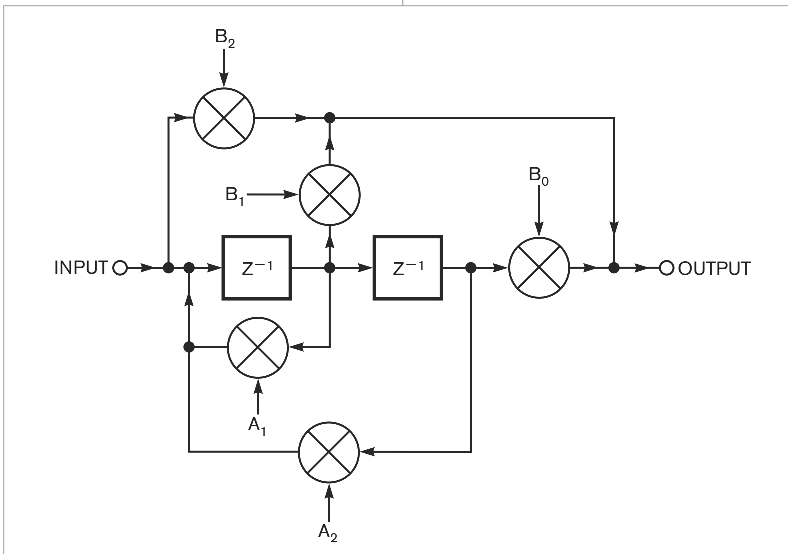

Figure 1 The transfer function for a second-order recursive digital filter has coefficient values that yield a lowpass, highpass, band-reject, or bandpass-transfer function.

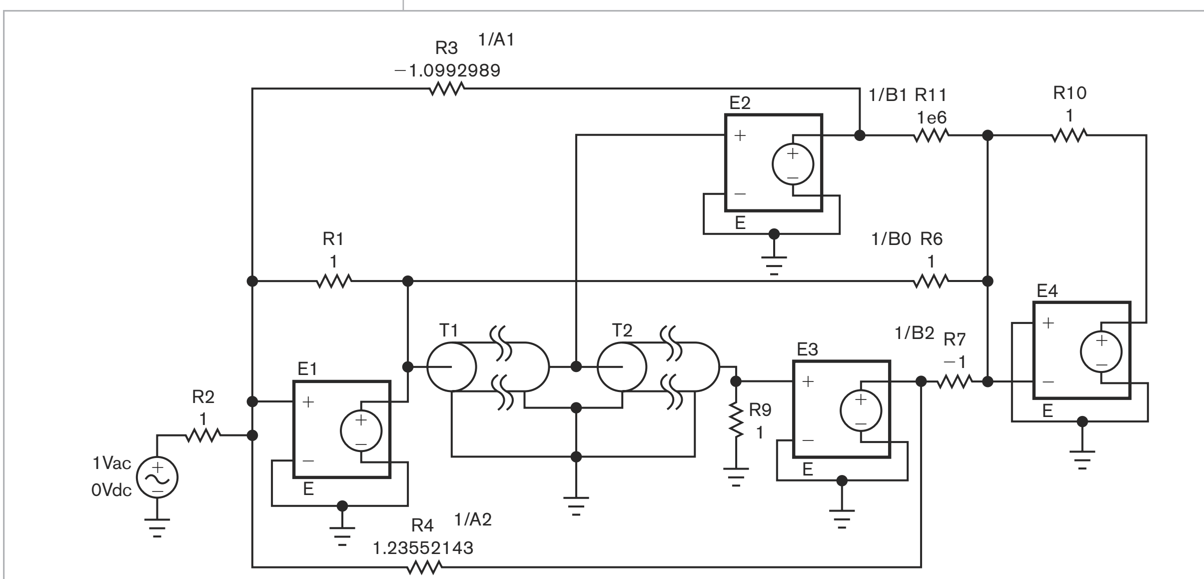

Figure 2 In the PSpice circuit, the VCVSs (voltage-controlled voltage sources), E1 and E2, simulate voltage followers, and VCVSs E3 and E4 and the resistors that connect to them simulate summers.

In this case, the transmission-line delay is 1/6000=166.67 μsec. If you additionally specify an impedance, Z, of 1Ω for the transmission line, then the parameters for the transmission line are Z_0=1Ω, and t=166.67 μsec. **Figure 2** shows the PSpice circuit. The VCVSs (voltage-controlled voltage sources), E1 and E2, simulate voltage followers, and VCVSs E3 and E4 and the resistors that connect to them simulate summers. **Figure 3** shows the results of the simulation.EDN

REFERENCE

1 López, David Báez, "Windows Based Filter Design with Winfilters," *IEEE Circuits and Devices*, Volume 13, 1997, pg 3.

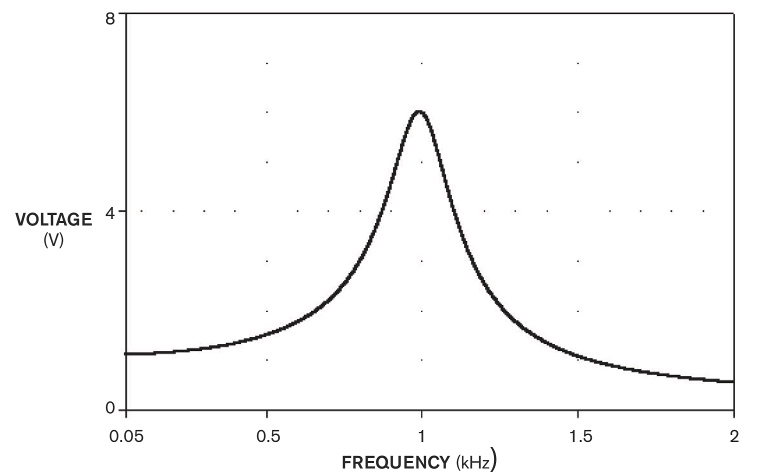

Figure 3 In this PSpice simulation, the digital bandpass filter uses transmission lines as delay lines.

Dual flip-flop forms simple delayed-pulse generator

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

Some applications require clock-timing adjustments, such as generating precision clocks for time-interleaved ADCs, or delay adjustments in a variety of precision-timing and pulse-delay applications. This Design Idea describes a delayed-pulse generator using a dual-CMOS D-type flip-flop (**Figure 1**). The circuit provides precision time delays of a trigger-input pulse. A dc-control voltage selects a time delay within the full-scale range. When the rising edge of a pulse triggers the input, the circuit's output generates a pulse with its rising edge delayed by an amount equal to the selected time delay, T_D, plus a fixed inherent propagation delay T_{PD}. Also, a time constant, R_4C_2, determines the output pulse's width.

A precision dc source, I_O, and capacitor C_1 set the full-scale delay range. When Q_3 is off, the current source charges capacitor C_1, generating a linear-ramp voltage with slope equal to I_O/C_1. The delay is the time it takes for the ramp to rise from its initial voltage to the control-voltage value.

In this application, the ramp slope is 10 mV/1 μsec, so that the full-scale delay range is 256 μsec for a control voltage of 0 to 2.56V. You can set the full-scale delay by changing I_O through either R_1+R_2 or capacitor C_1. For best accuracy, the current source can range from 10 μA to 1 mA, the capacitor's value can range from 1 nF to 1 μF, and the corresponding full-scale delay can range from 2.56 μsec to 256 msec. Use a precision film capacitor for C_1.

The basis of the current source is a shunt precision-micropower-voltage-reference, IC_3, producing a reference voltage of 1.233V with an initial ac-

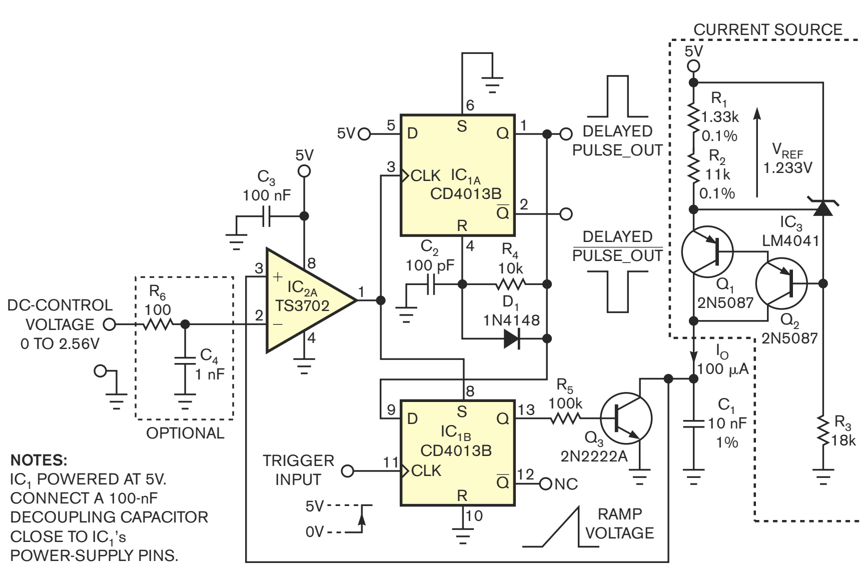

Figure 1 The rising edge of a trigger input starts a precision ramp voltage that compares with a control voltage, generating a precise delay.

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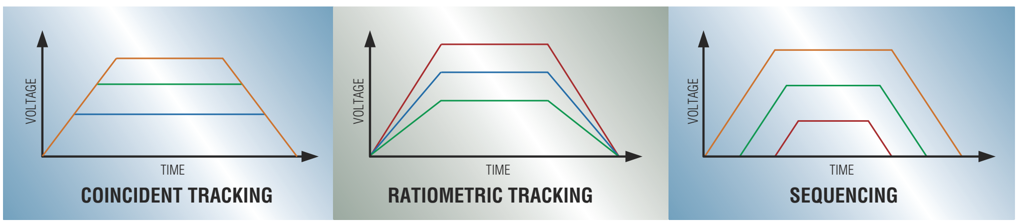

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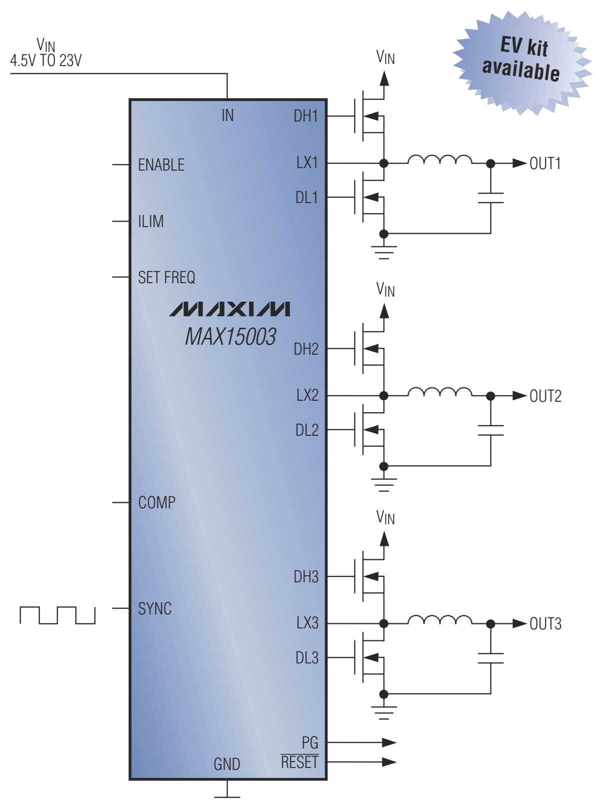
MAX15003	Triple	48-TQFN (7 x 7)



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IC_{1A} is a one-shot circuit (**Reference 1**). The output pulse's width, T_W, is $R_4C_2\times\ln(V_{DD}/V_{TH})$, where V_{TH} is the threshold voltage of the digital CMOS. Because $V_{TH}\approx V_{DD}/2$, then $T_W\approx R_4C_2\times 0.69$. Diode D_1 reduces recovery time. After power-up, Q_3 is in saturation, absorbing the current source's output, and, as soon as an input pulse triggers the circuit, IC_{1B}'s Q output goes low, switching off Q_3, starting a ramp. When the ramp exceeds the control voltage, then the IC_{2A} comparator's output goes high, and the rising edge triggers one-shot IC_{1A} and switches on Q_3 through IC_{1B}, allowing the discharge of the capacitor C_1. When an input pulse triggers the circuit, any other trigger pulse that occurs before the falling edge of the delayed output pulse does not produce an output pulse; in other words, the circuit is not retriggerable. This feature permits you, at the same time, to divide and delay an input-trigger clock.

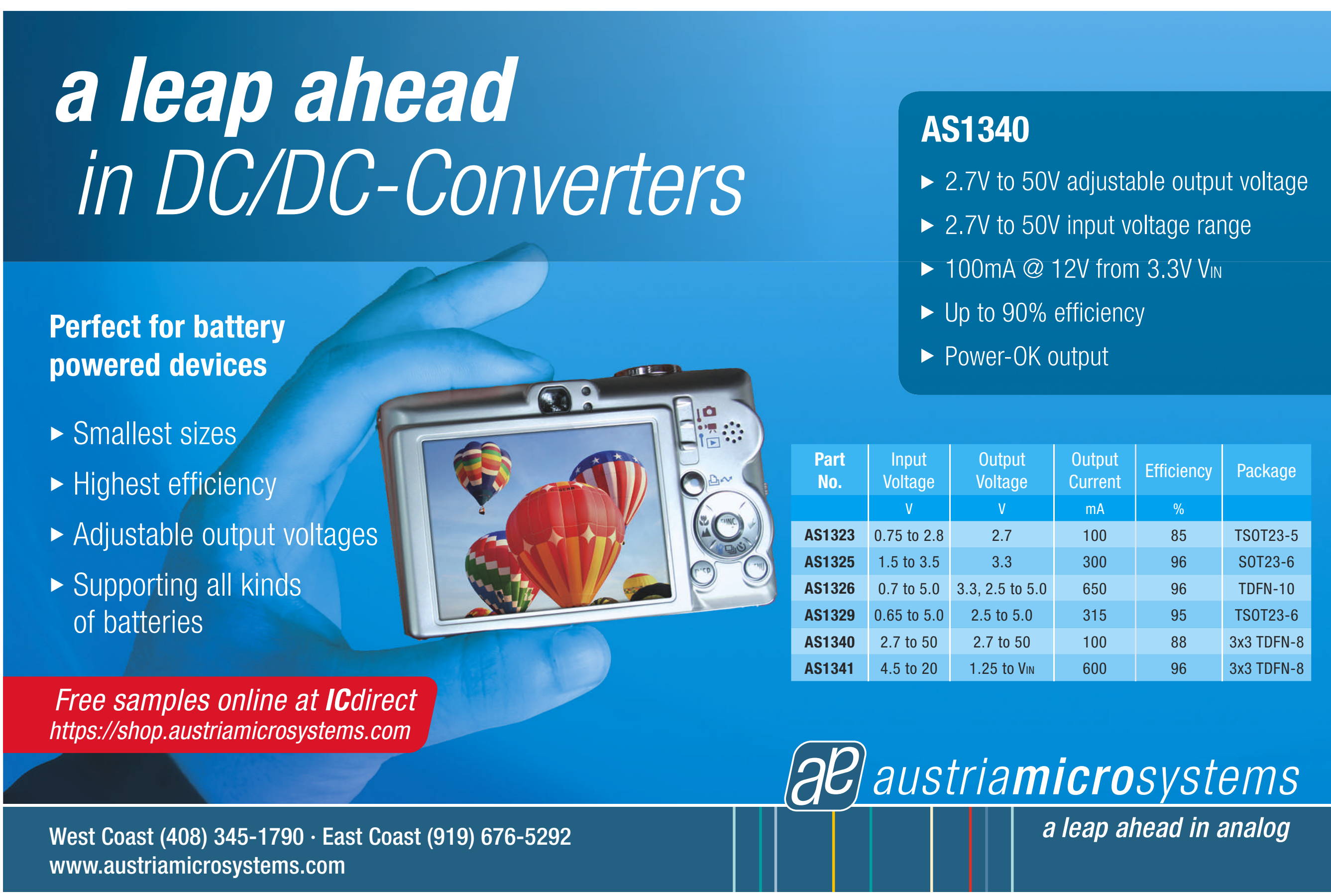
Although IC_1 and IC_2 can operate from a 3 to 16V supply, the minimum supply voltage of the circuit is 5V; otherwise, Q_1 and Q_2 approach saturation, generating to a less linear ramp voltage. Voltage comparator IC_{2A}, an STMicroelectronics (www.st.com) TS3702, has an input-common-mode-voltage range that includes ground, permitting you to monitor input voltages as low as 0V.

However, for correct operation of the circuit, the minimum control voltage must be greater than the saturation voltage of Q_3. For the components in **Figure 1**, the measured value is 12 mV. If you want to reduce this voltage, you can use a digital N-channel MOSFET with low on-resistance. The optional input lowpass filter, comprising R_6 and C_4, helps to clean noise from the dc-control voltage.

If a DAC drives the control input, you can build a digitally programmable delay generator. A suitable low-cost, 8-bit DAC is the AD558 from Analog Devices (www.analog.com), which features an internal precision bandgap reference to provide an output voltage of 0 to 2.56V, making 1 LSB equal to 1 μsec. It operates from 5 to 16V, with a 1-μsec settling time. The circuit's quiescent current, I_{DD}, is less than 300 μA because all ICs are micropower. **EDN**

REFERENCE

1. Bhandarkar, Santosh, "Single-IC-based electronic circuit replaces mechanical switch" *EDN*, March 15, 2007, pg 76, www.edn.com/article/CA6421439.



productroundup

CIRCUIT PROTECTION

Protection controller disconnects during wall-adapter overvoltage

Suiting USB charge protection in portable and consumer devices, the NCP361 overvoltage-protection controller uses an internal P-channel FET requiring no external devices. In the event of overvoltage from a wall adapter causing the input voltage to exceed the overvoltage shroud, the controller disconnects the output from the input, protecting the downstream system. Features include a 20-μA current consumption, a 750-mA typical overcurrent protection, and an improvement in VBUS protection of as much as 20V compared with discrete zener-based devices. A negative-going flag output alerts the system when a fault occurs, and an enable pin can force the device to an off-state. Available in a 2×2-mm uDFN- package, the NCP361 overvoltage-protection controller costs 40 cents (3000).

On Semiconductor, www.onsemi.com

ESD-protection diode comes in a small package

The ESD0201 SMD ESD (electrostatic-discharge)-protection TVS (transient-voltage-suppression) diodes provide 30-kV contact-discharge ESD levels, according to IEC61000 standards. The diodes feature 20-pF input capacitance and 10V clamp voltage, reducing IC latch-up and soft errors. Measuring 0.02×0.01 in., the ESD0201-01FR TVS diode costs 7 cents (25,000).

OnChip Devices, www.onchip.com

Solid-state protection devices meet a variety of IEC standards

Adding to the vendor's RailClamp solid-state protection-device family, the RClamp0524J 5V protection device aims at DisplayPort and other high-speed applications. Providing a 0.3-pF capacitance, the protection device meets IEC 61000-4-0 standards for ESD protection, including ±15-kV for air and ±8-kV for contact. The device also meets EFT (electrical-fast-transient)

and lightning-strike IEC standards. Measuring 2.7×1×0.58 mm in a SLP2710P8-8 package, the RClamp0524J costs 35 cents (1000).
Semtech Corp, **www.semtech.com**

Devices combine EMI filtering and ESD protection in small packages

Combining EMI filtering and ESD (electrostatic-discharge) protection, the EMIF01-1003M3, and EMIF02-1003M6 meet IEC61000-4-2 level 4 for ESD protection and provide a 30-pF line-to-ground capacitance. The EMIF01 and EMIF02 provide 9 and 17V clamping voltages, respectively, at a 15-kV ESD strike. The single-line EMIF01-1003M3 measures 1×0.6×0.6-mm in a SOT883 package; the EMIF02-1003M6 measures 1×1.45×0.55-mm with a 0.6-mm^2 footprint and comes in a lead QFN-6 package. The EMIF01-1003M3 and EMIF02-1003M6 cost 9 and 15 cents (100,000), respectively.
STMicroelectronics, **www.st.com**

Low-capacitance diode-array family targets handheld devices

Aiming at portable, handheld systems, this family of low-capacitance diode-array devices provides ESD (electrostatic-discharge) and clamping protection. The devices use the vendor's TVS^2 (transient-voltage-protection using trench-vertical-structure) device and process technology. Features include ±30-kVESD protection for contact and air discharge, 6.9V maximum channel-clamping voltage at 15A peak-pulse current, and 15-pF typical capacitance. The single-diode AOZ8201 and AOZ8211 come in 1.6×0.8×0.6-mm SOD523 and 1×0.6×0.4-mm SOD923 packages, respectively. Measuring 1.6×1.6×0.6 mm, the four-channel AOZ8204 and five-channel AOZ8205 diode arrays come in SC-89 housing. The AOZ8201, AOZ8204, AOZ8205, and AOZ8211 devices cost 8.2, 10.3, 12.1, and 9.9 cents (1000), respectively.
Alpha & Omega Semiconductor, **www.aosmd.com**

EMBEDDED SYSTEMS

Digital-bit-stream card uses one to 16 channels at 125 MHz

The UF2e-7005 digital-bit-stream card has 16 channels that can be set to input or output with a 125-MHz maximum clock rate. The PCIe (PCI Express) card uses one, two, four, eight, or 16 channels while using all of the available card memory. The card comes with 64 Mbytes memory, expandable to as much as 4 Gbytes, and enables the recording or generating of signals for 16-sec periods on 16 channels at 125 MHz or for 262-sec periods on one channel at 125 MHz. The UF2e-7005 card costs $2590.
Strategic Test, **www.strategic-test.com**

productroundup

EMBEDDED SYSTEMS

Gigabit Ethernet switch family supports full-wire-speed L2 bridging

Targeting embedded-system applications, the ComEth4070a family of 6U VME L3 Gigabit Ethernet switches uses a Gigabit-switch engine and a PHY (physical)-layer transceiver. The switches combine a Layer 2+ switch and a Layer 3 router on a single board. The device supports full-wire speed L2 bridging and IP (Internet Protocol) routing with L2-L4 Access List for classification, filtering, and prioritization. Combining queue-priority-eight levels with QOS (quality-of-service) polecat allow tuning of jitter in critical applications. The device also provides 24 Gigabit Ethernet ports with 37 millions-packet/sec switching capacity. Devices in the ComEth4070a family cost $5200 each.

Interface Concept, www.interfaceconcept.com

Wireless RS-232-to-USB transceiver connects to any RS-232 device

This wireless RS-232-to-USB transceiver interfaces and makes wireless any RS-232 device. The wireless-receiver module connects to a computer through a USB interface, allowing communication with the RS-232 device. The transceiver costs $159.

Omega Engineering, www.omega.com

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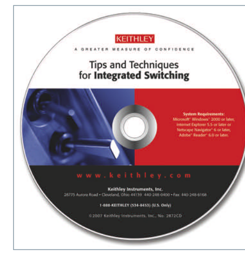

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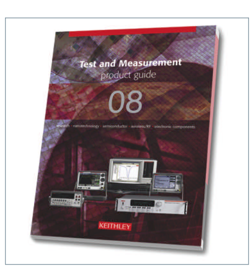

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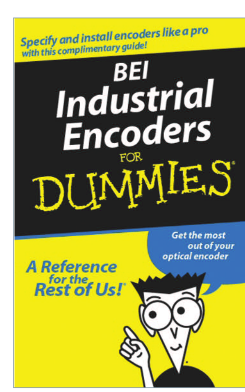

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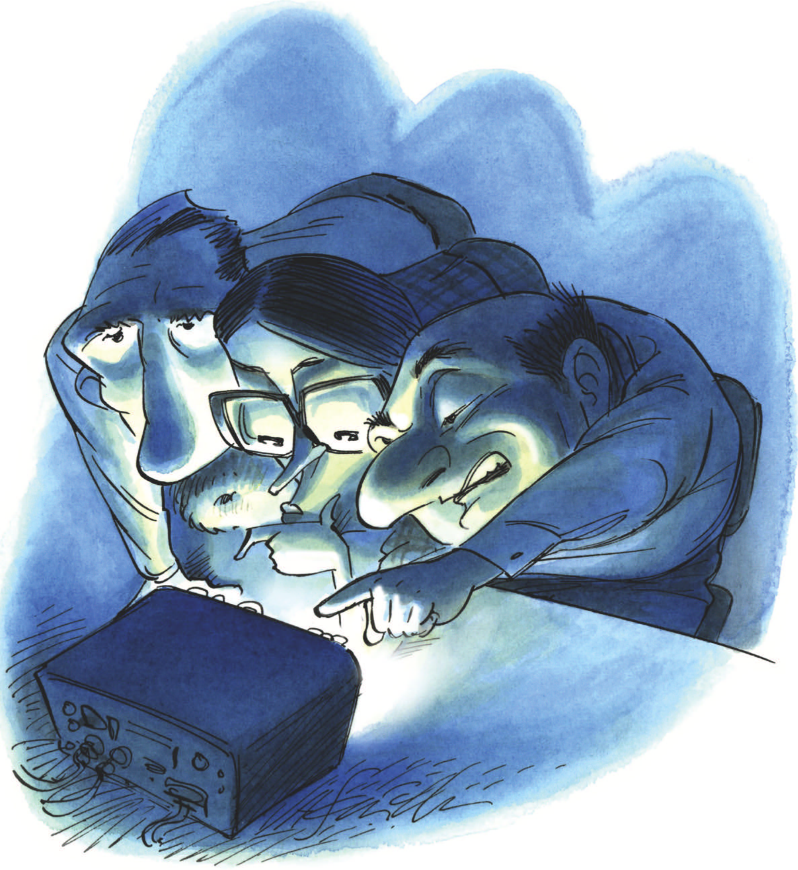
Finding clock glitches



DANIEL VASCONCELLOS

It was a dark and stormy night. It was dark because we had turned off all the lights in the lab as we anxiously studied the bright-blue-green glow of the oscilloscope, and it was stormy because our prototypes were not cooperating with our troubleshooting efforts, and the boss was getting antsy. (Note that "antsy" is an anagram of "nasty.")

The previous Friday afternoon, all had been working great. Four of our brand-new babies were finally debugged, tucked safely into their card slots, and obediently passing error-free bits back and forth over the backplane and across the optical links. We went home with big smiles and plans for a weekend celebration, thinking that the project was near completion.

On Monday morning, the bit-error counters had climbed to record numbers and were steadily increasing. All the optical-link SNRs (signal-to-noise ratios) were great, but each card insisted on periodically, randomly, and independently flipping bits. The following days of troubleshooting efforts concentrated on the analog optical links. Who ever heard of digital circuits giving this kind of trouble? Digital circuits either work, or they don't, right?

After chasing down many blind alleys, late one night we finally looked at the buffered-system clock and backplane data on the scope—a Tektronix dual-channel analog job with a nice, bright CRT screen. In the dark of the lab, one sharp-eyed colleague looked at the clock trace and said, "What's that?" A little smudge of light had appeared where none belonged.

Cranking up the timebase and vertical scale to position the brightest trace portions off screen (but still with a phosphor glow from reflected electrons), we were able to just discern the ghost of something that was not right. Just after the clock's falling edge, we observed an occasional small pulse, made very faint by its infrequent occurrence. Bingo!

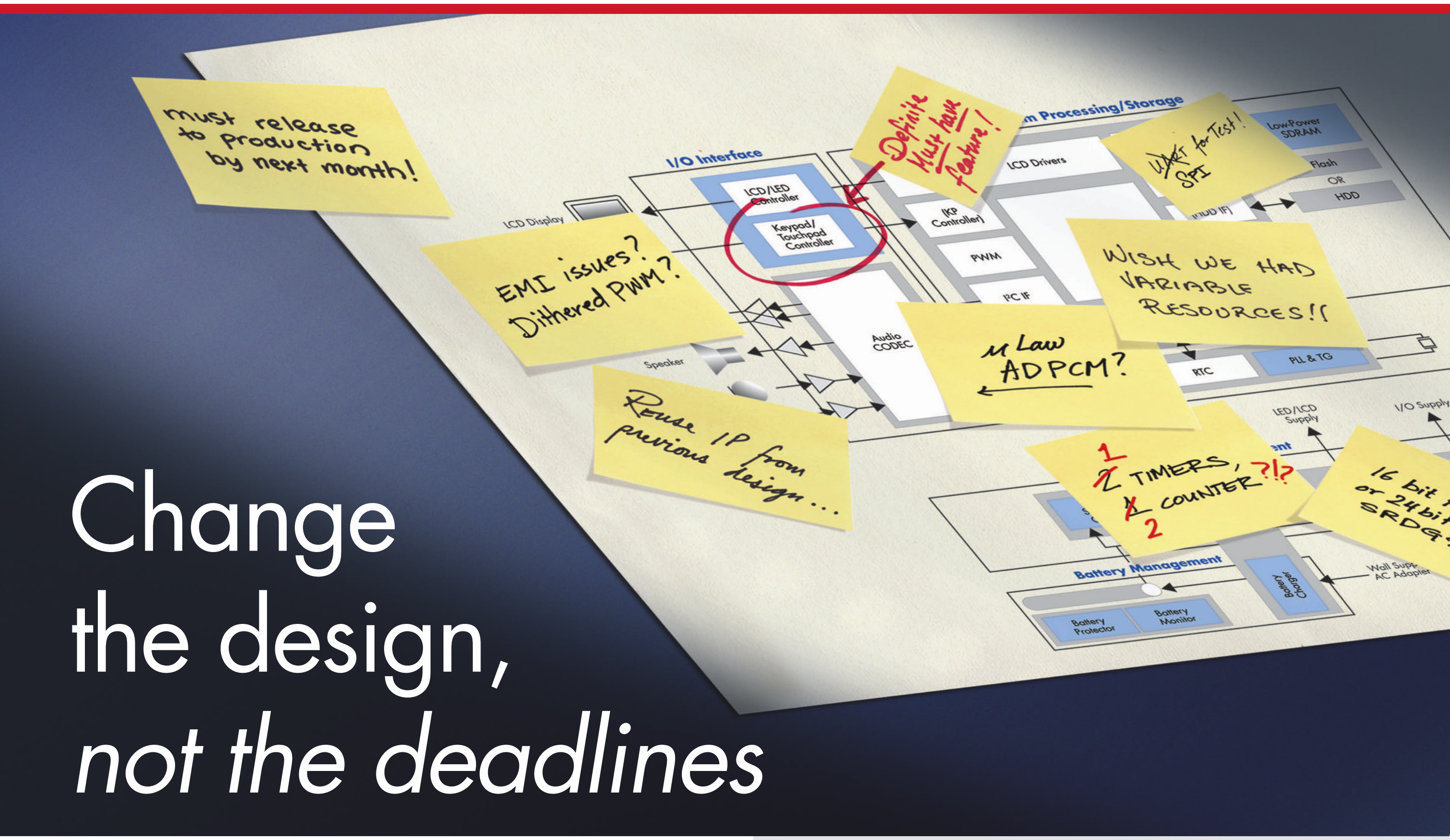
FINDING PROBLEMS LIKE THIS TOOK A LOT OF EFFORT AND PERSEVERANCE, COMBINED WITH GOOD EYESIGHT AND A DARKENED LAB AT NIGHT.

Today, a digital scope set to "runt trigger" or "infinite persistence" would have immediately found this problem, but analog scopes from back then did not have those features. Finding problems like this took a lot of effort and perseverance, combined with good eyesight and a darkened lab at night.

It turned out that placing the card's backplane interface buffers 3 in. away from the connector formed stubs. As more and more of these cards loaded the parallel backplane bus, the problem got worse. The backplane clock edges were ringing under the stub loading to the point at which the ringing occasionally passed the buffer's digital threshold and added an extra clock cycle.

We respun the card, and it worked great. EDN

Glen Chenier is a former telecom engineer and is now a design consultant. You can reach him at glen@teetertottertreestuff.com. Like Glen, you can share your Tales from the Cube and receive $200. Contact edn.editor@reedbusiness.com.



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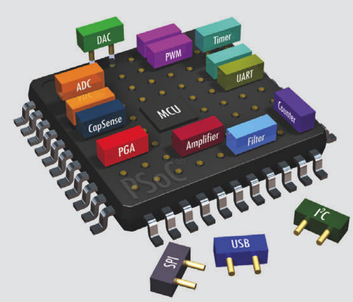

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